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UNITED STATES DISTRICT COURT
NORTHERN DISTRICT OF CALIFORNIA

RICOH COMPANY, LTD., Plaintiff, vs. AEROFLEX ET AL, Defendants.	**CASE NO. CV 03-4669-MJJ (EMC)** **Consolidated with** **CASE NO. CV 03-2289-MJJ (EMC)** **DECLARATION OF MICHAEL WEINSTEIN IN SUPPORT OF RICOH'S OPPOSITION TO DEFENDANTS' MOTION FOR PARTIAL SUMMARY JUDGMENT** **Date: November 1, 2005** **Time: 9:30 a.m.** **Courtroom: 11**
SYNOPSYS, INC., Plaintiff, vs. RICOH COMPANY, LTD., Defendants.	

Michael A. Weinstein declares as follows:

1. My name is Michael A. Weinstein, an attorney with the law firm of Dickstein, Shapiro, Morin & Oshinsky, LLP, counsel for Ricoh Company, Ltd. ("Ricoh"). I am over the age of 21 and am competent to make this declaration. Based on my personal knowledge and information, I hereby declare to all the facts in this declaration

2. Discovery yet to be meaningfully produced includes the identification of who is performing the logic synthesis on the ASIC defendants' products.

3. Discovery yet to be meaningfully produced includes the identification of all of the details regarding the inputs, logic synthesis, and outputs as used by the ASIC defendants, or someone on their behalf.

4. Discovery yet to be meaningfully produced includes the source code for all of the versions of logic synthesis programs used by the defendants in performing the logic synthesis process that are accused of infringing the '432 patent.

5. Discovery yet to be meaningfully produced includes detailed manuals explaining defendants, or someone on their behalf, production operation relating to the process of using all of the versions of the logic synthesis software.

6. Discovery yet to be meaningfully produced includes internal guides and procedure manuals for manufacturing the defendants' ASICs when using all of the logic synthesis systems.

7. Discovery yet to be meaningfully produced includes the identification of all of products and libraries the defendants, or someone on their behalf, use in performing the logic synthesis processes.

8. Discovery yet to be meaningfully produced includes the identification of where defendants, or someone on their behalf, perform the logic synthesis process.

9. Discovery yet to be meaningfully produced includes the identification of which companies and where the remaining portions of the manufacturing of the defendants' ASICs is done.

10. Discovery yet to be meaningfully produced includes documents showing the operation flow and connection between the logic synthesis and the use of the output in the subsequent steps in the manufacturing process of the Defendants' ASICs.

11. Discovery yet to be meaningfully produced includes the activities of the defendants in carrying out and/or directing the steps of the manufacture of the chips from initial input into the design portion of the operation through the final output of the completed ASIC.

12. The ASIC defendants are refusing to provide meaningful document discovery until mid October, and to date have refused to schedule any depositions at all.

13. Ricoh has served on each of the defendants discovery requests seeking the information relating to the above paragraphs 2-11.

14. Attached hereto as Ex. 1 is a true and correct copy of British Patent No. 1 445 914, cited as prior art in the '432 patent.

15. Attached hereto as Ex. 2 is a true and correct copy of excerpt from PowerPoint presentation used by counsel for Synopsys and ASIC defendants during their Markman arguments on Dec. 15, 2005, the relevant portion of which was as prepared by their expert Dr. Kowalski

16. Attached hereto as Ex. 3 is a true and correct copy of excerpts from Yanda, Heynes & Miller, *Demystifying Chipmaking* (Elsevier 2005)

17. Attached hereto as Ex. 4 is a true and correct copy of the deposition transcript of Michael S. Heynes of July 27, 2005.

18. Attached hereto as Ex. 5 is a true and correct copy of *AT&T Corp. v. Microsoft Corp.*, 2004 WL 406640 (S.D.N.Y. 2004), *aff'd,* 414 F.3d 1366 (Fed. Cir. 2005).

19. Attached hereto as Ex. 6 is a true and correct copy of U.S. Patent No. 4,922,432.

20. Attached hereto as Ex. 7 is a true and correct copy of the deposition transcript of Edward Dwyer of February 3, 2004 (designated confidential by counsel for the ASIC defendants and Synopsys).

21. Attached hereto as Ex. 8 is a true and correct copy of the declaration of Ricoh's expert V. Thomas Rhyne of February 24, 2004.

22. Attached hereto as Ex. 9 is a true and correct copy of excerpts from Heynes & Miller, *Integrated Circuit Manufacturing Synopsis* (Semiconductor Services 3d ed. 2002)

23. Attached hereto as Ex. 10 is a true and correct copy of the deposition transcript of V. Thomas Rhyne of April 14, 2004.

24. Attached hereto as Ex. 11 is a true and correct copy of the declaration of Ricoh employee Takamitsu Yamada of February 6, 2004.

25. Attached hereto as Ex. 12 is a true and correct copy of the deposition transcript of Synopsys employee Eric Olson of August 2, 2005.

26. Attached hereto as Ex. 13 is a true and correct copy of excerpts from Design Compiler User Guide v.2003.12.

27. Attached hereto as Ex. 14 is a true and correct copy of excerpts from Chip Synthesis Workshop – Lab Guide (designated confidential by Synopsys).

I declare under penalty of perjury under the laws of the United States of America that the foregoing is true and correct. Signed at Washington, D.C. on August 23, 2005.

/s Michael A. Weinstein
Michael A. Weinstein

PATENT SPECIFICATION

(11) 1 445 914

1 445 914

(21) Application No. 37953/74 (22) Filed 30 Aug. 1974
(31) Convention Application No. 401 303
(32) Filed 27 Sept. 1973 in
(33) United States of America (US)
(44) Complete Specification published 11 Aug. 1976
(51) INT CL² G06F 15/20
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(19)

(54) IMPROVEMENTS RELATING TO APPARATUS FOR PRODUCING GRAPHICAL DATA DESCRIPTIVE OF AN INTEGRATED CIRCUIT DESIGN

(71) We, INTERNATIONAL BUSINESS MACHINES CORPORATION, a Corporation organized and existing under the laws of the State of New York in the United States of America, of Armonk, New York 10504, United States of America, do hereby declare the invention, for which we pray that a patent may be granted to us, and the method by which it is to be performed, to be particularly described in and by the following statement:—

This invention relates to apparatus for producing graphical data descriptive of integrated circuit semiconductor chip design. It is concerned in improving the design of semiconductor chips by means of design automation techniques to produce chip design data that may be used to control machines which make photolithographic masks used to manufacture the semiconductor chips.

The use of design automation for making large scale integrated (LSI) chips and the advantages thereof are disclosed in "Computer", Vol. 5, No. 3 pages 18—52, published by the IEEE Computer Society and in the complete Specifications of our copending Applications for Letters Patent Nos. 25812/73 and 58461/72 (Serial Nos. 1 414 018 and 1 405 508 respectively. LSI devices can be generally classed as "non-random" and "random" types. A "non-random" LSI device is characterized by an array of duplicate circuits such as might be used in a memory device or a read-only store (ROS). A "random" LSI device is characterized by the lack of any repetitive uniformity of circuits on a chip. The circuits, and functions performed thereby, may vary on a single chip. An example would be a chip containing combinational and sequential logic for use in the control section of a computer. Quite obviously, designing random LSI chips is a difficult task and it is within such an art that design automation techniques are particularly advantageous and it is the general area which the present invention improves.

Before the invention is explained in detail a general design process will be described. A prerequisite to making a given device is the existence of a given technology in which the process of making the device is established and the electrical characteristics of the circuits and packaging are known. Design criteria or rules for the technology are established. With the knowledge of such rules, a chip designer performs the complex task of translating logical functions to be performed in a system into actual physical LSI devices that perform the functions. To do this, the designer interacts with and is aided by a design automation (DA) system. The theory for use of any DA system is that there are many operations which are subject to algorithmic analysis and control which can be best done by a computer while there are other functions that require human skill to be performed effectively or best. In designing random type LSI chips, a chip designer is "best" at deciding what functions, and circuits to perform such functions, are to be placed on a given chip and where elements should be generally placed. A chip designer can place many relatively small diverse functions on a given chip or he may break up a function and place it on different chips. The chip designer produces an output that is partially descriptive of a chip. This output is fed as an input to a DA system which performs its functions to provide an output that is used to control the physical process of making the LSI device. This would entail making photolithographic masks.

In the design process there are two mutually exclusive techniques, "free form" design and "rules driven" design. The

former technique is unrestricted and characterized by efficient silicon or chip utilization but has a long design cycle (e.g., three to six months) and requires manual checking. The latter technique is restricted and characterized by a fast design cycle (e.g., two to four weeks) and automatic checking but may produce inefficient silicon utilization.

A specific example of the restricted "rules driven" technique used in connection with FET (field effect transistor) LSI devices is disclosed in the aforementioned complete Specification of our Application for Letters Patent No. 58461/72 (Serial No. 1 405 508). In accordance with such "rules driven" technique, the metallization areas, diffusion areas, power and signal busses, I/O pads and FET devices are laid out on an orthogonal grid pattern in accordance with relatively rigid or restricted rules, whereby the maximum use can be made of the DA system to provide a fast design cycle.

An object of the present invention is to provide an apparatus that combines both "free form" and "rules driven" techniques.

According to the invention, apparatus for producing graphical data descriptive of an integrated circuit design comprises first means adapted to store graphical descriptions of freeform designs, second means adapted to store topological data and electrical characteristics of rules restricted designs, means adapted to enter information denoting the location and relationship of a freeform design to a rules restricted design, means adapted to generate a graphical description of said rules restricted design, and means adapted to merge the generated graphical description of said rules restricted design with the graphical description of said freeform design stored in said first means to form said graphical data descriptive of an integrated circuit design.

In the embodiment to be described below, a library of predesigned graphical descriptions that describe circuits designed by the free form technique is stored within the design automation system. A chip designer would design the layout of a chip including both "free form" and "rules driven" portions. An input is fed to the DA system which specifies the rules driven design in the established manner and specifies the free form design by defining the library description thereof, and the relative placement of the design on the chip. The system in response to such input generates a graphical description of the rules driven design without doing any automatic checking of the internal connections etc of the free form design. The generated description or topology is then merged with the free form description or topology from the library to form a complete chip description from which is derived data for making photolithographic masks.

The invention will now be particularly described, by way of example, with reference to the accompanying drawings, in which:—

Figure 1 is a general flowchart showing the overall design process,

Figure 2 is a general flowchart showing the overall chip design process of Figure 1 in more detail,

Figure 3 is a diagrammatic layout of a chip design providing an example useful in understanding the invention,

Figure 4 is a more detailed flowchart,

Figures 5a to f illustrate various descriptive data related to the example shown in Figure 3, and

Figure 6 is a general flowchart summarizing the steps in the design process.

Referring now to Figure 1, in accordance with the overall or general process, a chip designer provides an input to a chip design system 10, the details of which will be discussed hereafter. The input of the chip designer incorporates both free form data for achieving efficient silicon utilization and incorporates rules driven data for taking maximum advantage of the speed and efficiency of the chip design system 10. The output of chip design step 10 is a graphical language description 11 of the eventual chip design. This description is fed as an input to a language processor 12 that provides an output for controlling the operation of an artwork generator 13 used to produce the masks for making the actual physical LSI chip. This overall process is disclosed in the aforementioned complete Specification of our Application for Letters Patent 58461/72 (Serial No. 1 405 508). A difference is that the chip design system 10 is modified and the addition of the freeform input by the chip designer.

Referring now to Figure 2, at the start of the process, the chip designer would provide input information 14 to the FET automated design system (FADS) 16. To do this, the designer, with knowledge of the functions to be incorporated into a chip, selects the desired circuits and devices from those available to him within the given technology, including those designs that are rules driven and those that represent a freeform design. The chip designer would ordinarily work with a graphical layout of the chip, such as illustrated in FIG. 3, which includes an image of the general grid structure including the power busses and I/O pads. Upon this layout, the designer would then

place the respective circuits. Stored within the system is a book library 18 which is a file of technology data describing the electrical characteristics of circuits, topology thereof and the images. The exact or specific information would be dependent upon the functions to be performed by the system which can vary from system to system. The information in the library may be divided into three types of books or collections of data. Types 1 and 2 respectively represent circuits that are specified by formulae so that the system calculates devices, shapes and locations, or may specify standard circuits conforming to the given rules. The third book type would be those providing the freeform topology.

Let us consider now in a little more detail the process used by the chip designer. The chip designer might first layout in a block diagram form the logical functions to be included within the chip as, for example, through the use of And and Or blocks. This would be the logic representations of the functions to be eventually created and performed within an actual chip. Next, the chip designer would select a chip image such as that shown in FIG. 3 and beging a layout of the various circuits to be included. He would first determine what devices or circuits are necessary to perform the logic functions and then would begin relative placement of these devices on the chip image. In the illustrated example, the chip image has 48 terminals and a bus network that divides the chip into four active areas in the form of columns or bays. A given circuit would be generally located in one of these bays. Also, the designer would decide which relative row of a given bay the circuit should go in, the relative row being the degree of vertical stacking of circuits within a given bay. This process is known as a placement of the devices on the image. Later, FADS 16 will determine exact placement. The relative placement can be done by assigning XY coordinates to the chip image which XY coordinate might for example, by convention, be considered to be the location of the lower lefthand corner of any given area of diffusion, contact, or metallization. Through use of the chips designer's skill, the various functions would be implemented within circuits and would attempt to provide maximum efficient use of the active area of a chip. The input information 14 is then generally divided into two aspects. The first is that connected with the description of the logic in accordance with the rules of the system and the second would be the description identifying the freeform device and its location and orientation.

FADS 16 is constructed in accordance with standard DA techniques and comprises a series of DA programs that are loaded in and executed on a general purpose computer such as a Model 158 of IBM (Registered Trade Mark) System/370. The language of the program can be any general programming language such as PL/1 which act upon the data provided by the graphical programming language to produce the design of the chip. In general, FADS 16 would, using input data 14 and information from library 18, construct an image of the circuits on the chip, except for the freeform, and convert any relative placements of the input into exact placements. The freeform itself would be treated as an area which has signal and power terminals to be accounted for, but the FADS system would do no internal checking of the freeform design to see that it worked. In other words, it would be the responsibility of the designer to make certain that the freeform design operated correctly. When FADS 16 has completed its processing, the result is output 20 which contains a partial description of the chip design for the rules design portion thereof, along with an identification of the freeforms to be incorporated. This partial chip description is then fed through a merge process 22.

Freeform identification of output 20 is used to obtain from library 18 the freeform description which in the merge process 22 is combined with the partial description from the output 20 to form a total chip description or graphical language description 11.

In the beginning of the design process, the chip designer would select a chip image layout on which to begin placing the various circuits and devices. Such a layout is shown in FIG. 3 which schematically illustrates a partially completed LSI chip 24. Such a device is constructed in accordance with the manner pointed out in the aforementioned Specification and generally comprises a silicon wafer having diffusions therein, such as 28, described in more detail below, forming part of the conductive pattern on the wafer and acting as part of the circuit devices. Two layers of thick and thin oxides are placed on top of the wafer and any metallization is done on top of the oxide layers. Contacts 30 provide vertical electrical connection between diffusion and metallization zones. It is to be understood that in a given technology system there might be several different images or basic images available to a designer that vary according to the number of I/O pads and chip size. In the illustrated chip 24, there are forty-eight I/O pads P1—P48 located around the periphery,

each pad being rectangular in shape and comprising metallization and diffusion. These pads are designed to be connected to external terminals for providing signals and power to chip 24. Thus, pad P1 is designed to power the substrate and it would include a contact leading from the upper metallization layer down to a diffusion area on the substrate. Pads P45 and P4 are designed to be connected to an external ground connection and are also connected to metallization busses GL and GR for providing a ground network on the left and right sides of the chip. Pads P21 and P28 are designed to be connected to voltage sources to provide main voltage busses MVL and MVR for the left and right sides of chip 24. Pad P22 is designed to be connected to a source of control voltage and is also connected to a control bus CV whereby a voltage applied to this bus will allow the circuits on the chip to be operated. Bus CV includes bifurcated arms extending parallel to busses MVL and MVR and having legs lying along each side of each bus in the manner pointed out in the above applications. The various vertical busses in the specific examples shown in FIG. 3 divide the active area of the chip into four columns in which the circuits and wiring are to be placed.

To illustrate the invention, FIG. 3 shows a rules design circuit CKT1 and a freeform or predesigned circuit CKT2. These circuits are shown merely for the purpose of illustrating the invention. In the case of the design of an actual chip, there would be many more circuits included to utilize the active area of the chip as effectively as possible. Circuit CKT1 is an FET device used to invert an output signal appearing from CKT2. CKT2 is a binary counter of conventional logic instruction having an input terminal BO1, and an output terminal ZO2. The function of the counter is to produce an output signal on the output terminal ZO2 upon receiving four input pulses or signals at input terminal BO1. Input terminal BO1 is connected by a network 101 to I/O pad P41. Output terminal ZO2 is connected by network 102 to the metal cap AO1 of CKT1. Diffusion rails 28 and 29 underlie cap AO1 but are separated therefrom by oxide layers. Rail 28 is connected via network 103 to I/O pad P36. The binary counter CKT2 is also provided with two power connectors PO1 and PO2 respectively connected to busses GL and MVL.

The flowchart of FIG. 4 is an expansion of FADS 16, Figure 2. Once the chip designer has completed the layout of the entire chip, the information can be translated into data that serves as an input to the FADS system. In general, there are four steps or operations in this system, the result of which is to produce the rules description 40 described above. Each step has an input from external information and from the output of a preceding step and each step provides partial information or generates a portion of the rules description 40, as pointed out in more detail hereafter. Within this diagram, while the various forms of external data input are shown schematically as coming from a punched card deck, it is to be understood that the input can be by any other standard input method associated with a data processing system. In general, as indicated previously, FADS 16 is designed primarily to handle the rules restricted design but is modified to recognize the existence of freeform designs.

The first function is chip image generation 38, the purpose of which is to allow the designer to select and, modify if he so desires, a standard image available to the system. The output of this step would include a description of such an image that would eventually be incorporated into the description 40. To obtain this output, three inputs are provided. The first input 32 identifies any part number and engineering change level associated with a given LSI chip 24. A second input 34 defines the basic image type to be used by the designer. The input can be information similar to that shown in FIG. 5f which includes a first field identifying the image and a second field identifying any particular columns where such a choice is available. Within this particular example, the image shown in FIG. 3 is a "default image" so designated in FIG. 5f, having four columns of active areas. A third type of input 36 provides an image description of the manner in which the basic image is to be modified for use by the designer if he so chooses. Such modifications might come about by bending the power busses. In the example, no modification is necessary.

The second operation 42 is to perform the functions of initial device sizing and data checking. The designer defines the logic to be implemented and the performance required from the logic. The system then calculates the device sizes required for each circuit to meet its specified performance. In general, the logic is described in terms of nets or grouping of circuit LSTs (logic service terminals) and I/O pads which must be connected to implement the logic function. Performance or speed requirements are indicated to the system by specifying the input waveform and/or capacitive loading present at the I/O pads and the performance of each circuit. During this operation, the system validates the designer's input and may perform a

number of checks including the following: each circuit has been equated to a book type; master logic list (MLL) is consistent with circuit data; fan-in to a circuit; number of outputs dotted; total fan-in to dotted circuits; load device has been specified for one circuit in a dotted net. It should be obvious that many of these checks are equated to only the rules restricted design and the checks are merely to make certain that the design conforms at least to certain ones of the rules checked for in this operation.

Operation 42, in addition to receiving as an input the output from the preceding step 38 receives a first input 44 called the pad spec or specification shown in detail in FIG. 5d. With reference to such Figure, the pad spec includes two fields for correlating the logical I/O numbers used by a designer to distinguish an I/O pad with an actual physical I/O pad number. The physical I/O number is optional and if the designer does not specify a particular one, the system will determine or specify one. In the particular example, the two physical pads P41 and P36 are also considered to be the same logical I/O pad numbers. The waveform field might be used to specify any special characteristics of a waveform. Where the field is not used, the pad is not a primary driver and receiver. The rise time specifies for example in nanoseconds the time of the rising input waveform where the pad is a primary input or has an off chip dot connection. In the example, it is assumed that the waveform associated with pad 41 has a rise time of 100 nanoseconds and fall time of 200 nanoseconds. The remaining field is the capacitance load expressed for example in picofarads, as seen by the circuit which is driving the I/O pad and should be specified if the I/O pad is primary output or has an off chip dot.

Another input to step 42 is MLL 48 shown in FIG. 5c. In general, the MLL describes the set of connection required to implement the desired logic. Each connection or net must be assigned a unique positive integer by the designer. The net is composed of two types of connections, circuit LSTs and I/O pads. The first field is the net number which in the particular example involves three nets numbered 101, 102 and 103. Next will come a series of paired fields identifying a circuit number and LST ID, the number of these fields being repeated for as many as are associated with a given net. A negative circuit number indicates an I/O pad, a positive number indicates an LST. For the specific example, shown in FIG. 3, FIG. 5c includes the specific or exemplary information shown.

The next input 46 to step 42 is the circuit data information as in Figure 5A, used to uniquely identify circuit blocks on the logic diagram and attach physical attributes to it and to specify circuit specifications or data in accordance with any terms defined within the associated book library. This data is initially supplied to step 42 without any placement information and is later modified to include the placement information as an input to a succeeding step as described below. The first column specifies the circuit number which in the example is 1. The next field identifies the book number which equates the circuit number to a logic function and topology stored in a book library 18. The next three columns or fields of column row and order are used to identify the relative placement of the circuit on the chip. In the example, the chip has four columns with the left column being numbered 1. The row refers to the relative vertical stacking within a given column where circuit 2 occupies the first row and circuit 1 occupies the second row. This is really relative and spaces may be skipped in between. The system will eventually determine the exact placement. Order refers to the number of circuits within a given row in a column and there may be more than one device although in the example, only one device AO1 is shown and this would have an order of 1. The next field orientation refers to the basic orientation as stored in the book library and whether it is to be mirror imaged about the X or Y axes. The remaining fields relate to certain circuit specifications or data which can be filled in or left blank in which case the default parameters would be used.

The remaining input to step 42 is freeform data 50 shown in detail in FIG. 5b. The first field identifies the circuit number. The next field identifies the book number which in this example is an arbitrary number 401 that would identify the associated topological and electrical characteristic information within book library 18. The X location and Y location would refer to the relative coordinates for the lower lefthand corner of the outline of circuit 2. The active area of the chip may be arbitrarily divided up into grid units each grid unit representing for example 0.025 microinches. The orientation of 1 indicates that it is to use the basic orientation within the book with no mirror imaging around the X or Y axes. This information is then used by the system to more or less outline or create a hole within which the processing relative to the other circuits proceed without any attempt to be made to check what is within the outline. The specific topology of the circuit is obtained

from the library as well as the locations of the terminals thereon so that the specification of the location of the corner of the circuit along with its orientation, is used to specify the location and also indirectly the geometry of the circuit.

The third operation 52 is one of circuit placement and this requires the designer to assign logic circuits to positions on the chip. The assignment is done in terms of relative coordinates which are automatically transformed to absolute coordinates by the system, the data or assignment being included as placement data 54 associated with the circuit data. This information is described previously relative to FIG. 5a wherein in step 54, the information enclosed in parenthesis is added.

The output from the circuit placement operation 52 includes a wire list 56 that indicates the coordinates for each LST which must be wired to implement the logic. It could also include any information for modifying the device size and delay that's based upon any revised loading or electrical parameters derived from the placement data. The chip designer would then utilize this wire list to produce an input 58 containing digit data information shown in FIG. 5e. the first field contains the net number corresponding to the same net number in MLL 48. The second field can be used to distinguish a code between whether the specifications are digitized on wiring channels or in grid units. The next three fields define the X, Y and Z coordinates for the starting point of the first line segment, the Z coordinate corresponding to the chip layer or mask level in which the wiring starts. The width field can be used by putting a zero therein to indicate that a standard width of metallization or diffusion is to be used or it can specify the actual width. The remaining fields, and there can be more than one dependent upon how many changes there are in the line segment, can be used to first define the direction of movement in either positive or negative X or Y direction from the starting point or a vertical direction and the steps field will specify the number of grid units or wiring channels along which the line segment will extend. If the direction is specified as indicating a change between layers, the steps field can then be used to specify a type of contact for accomplishing the change. The X and Y coordinates define the location of the wire or LST relative to the origin of the chip.

The final step 60 of the process is a wire routing operation that utilizes the digit data and output from step 52 to route wires to interconnect all the circuit LSTs and I/O pads. The wire routing step checks to see that the logical circuit LSTs coded in the MLL are matched against gates placed in the digitization. It also checks for net continuity, intersection nd critical spacing. The final output of the wiring routing step 60 is placed in 40 and completes the description of the chip except for the specific information stored in the book library describing the internals of the freeform design. With the design completed, various other tests such as delay calculations, may be performed to aid the designer and help ensure the accuracy of the completed design.

Referring now to FIG. 6, the overall steps in the design process are summarized in flowchart form. Initially, step 70 involves the predesign of those circuits associated with the rules restricted design. Step 72 involves predesigning the freeform designs and organizing the data into books. As indicated previously, the system will operate on the rules books 70 to perform as many DA functions relative thereto as possible whereas the number of functions performed on the freeform books 72 is restricted in that no checks are made by the automated design system relative to any of the internal workings of the devices. These predesigns are converted into data acceptable to the data processing system and, in step 74, they are stored within the system in books containing the topological data and electrical characteristics of the circuits and graphical descriptions of the freeform designs. Thereafter, step 76 generates the graphical description of the image, rules circuits and wiring, such graphical description of the freeform design being already stored in book form. Next, step 78, the description from step 76 is merged with the description of the freeform design as obtained from the library, the merger producing the graphical description of the total device. Thereafter, the appropriate photolithographic masks are made in step 80 for use in the step 82 to actually produce an LSI device.

WHAT WE CLAIM IS:—

1. Apparatus for producing graphical data descriptive of an integrated circuit design comprising first means adapted to store graphical descriptions of freeform designs, second means adapted to store topological data and electrical characteristics of rules restricted designs, means adapted to enter information denoting the location and relationship of a freeform design to a rules restricted design, means adapted to generate a graphical description of said rules restricted design, and means adapted to merge the generated graphical description of said rules restricted design with the graphical description of said freeform design stored in said first means

to form said graphical data descriptive of an integrated circuit design.

2. Apparatus as claimed in claim 1, wherein said entering means comprises means adapted to specify the relative location on said freeform design of signal and power terminals, and means adapted to specify conductive networks interconnecting said terminals with said rules restricted design.

3. Apparatus as claimed in claim 2 comprising means adapted to store topological information providing relative orientations of any design in the form of mirror images about Cartesian axes, and means adapted to specify the desired orientation of said freeform design.

4. Apparatus as claimed in claim 1, comprising means adapted to specify the location of said freeform design relative to an origin on said chip of a grid unit locating coordinates.

5. Apparatus as claimed in any preceding claim, comprising means adapted to store a graphical description of at least one image for said integrated circuit design defining the topology of power busses and input-output pads.

6. Apparatus for producing graphical data descriptive of an integrated circuit design, substantially as herein described with reference to the accompanying drawings.

JOHN BLAKE,
Chartered Patent Agent,
Agent for the Applicants.

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Published by the Patent Office, 25 Southampton Buildings, London, WC2A 1AY, from which copies may be obtained.

1445914 COMPLETE SPECIFICATION
6 SHEETS *This drawing is a reproduction of the Original on a reduced scale*
Sheet 1

FIG. 1

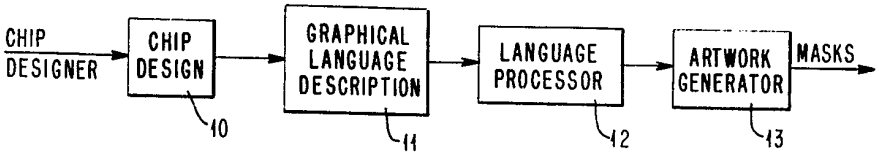
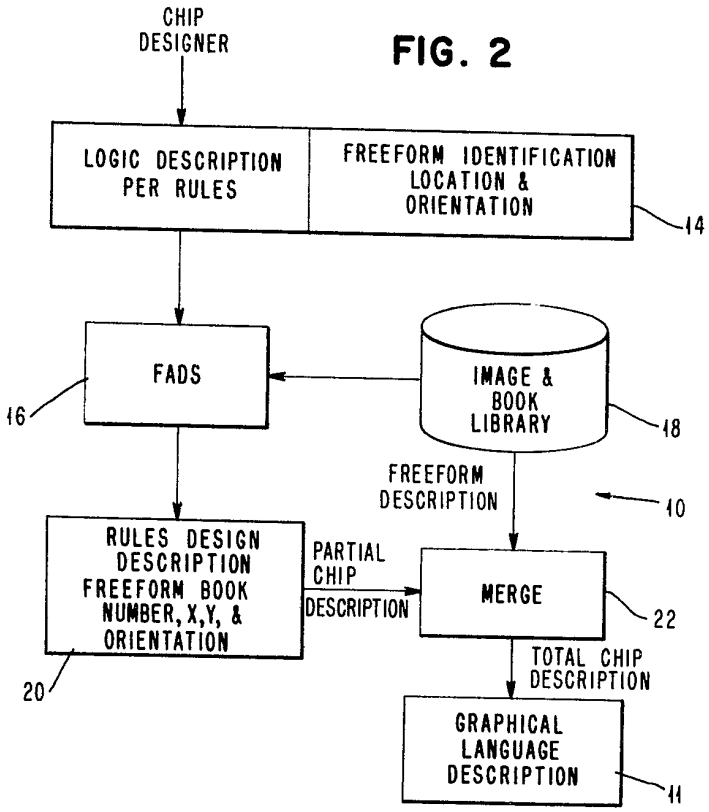
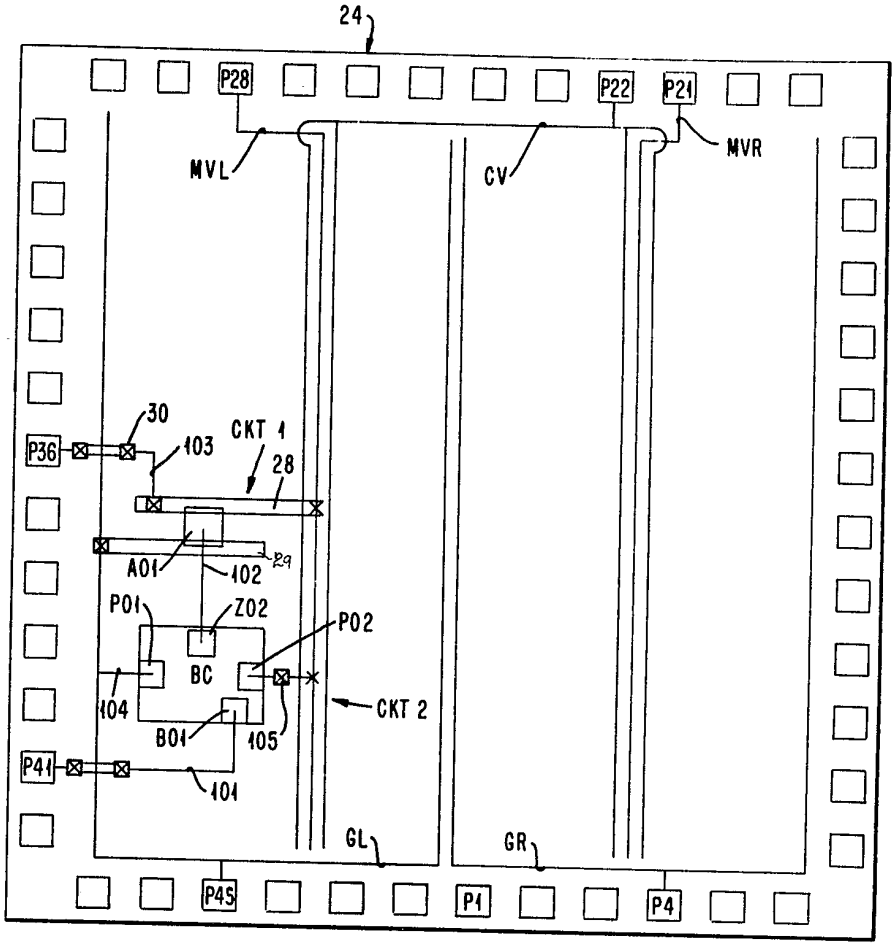


FIG. 2



1445914 COMPLETE SPECIFICATION
6 SHEETS This drawing is a reproduction of the Original on a reduced scale
Sheet 2

FIG. 3



1445914 COMPLETE SPECIFICATION
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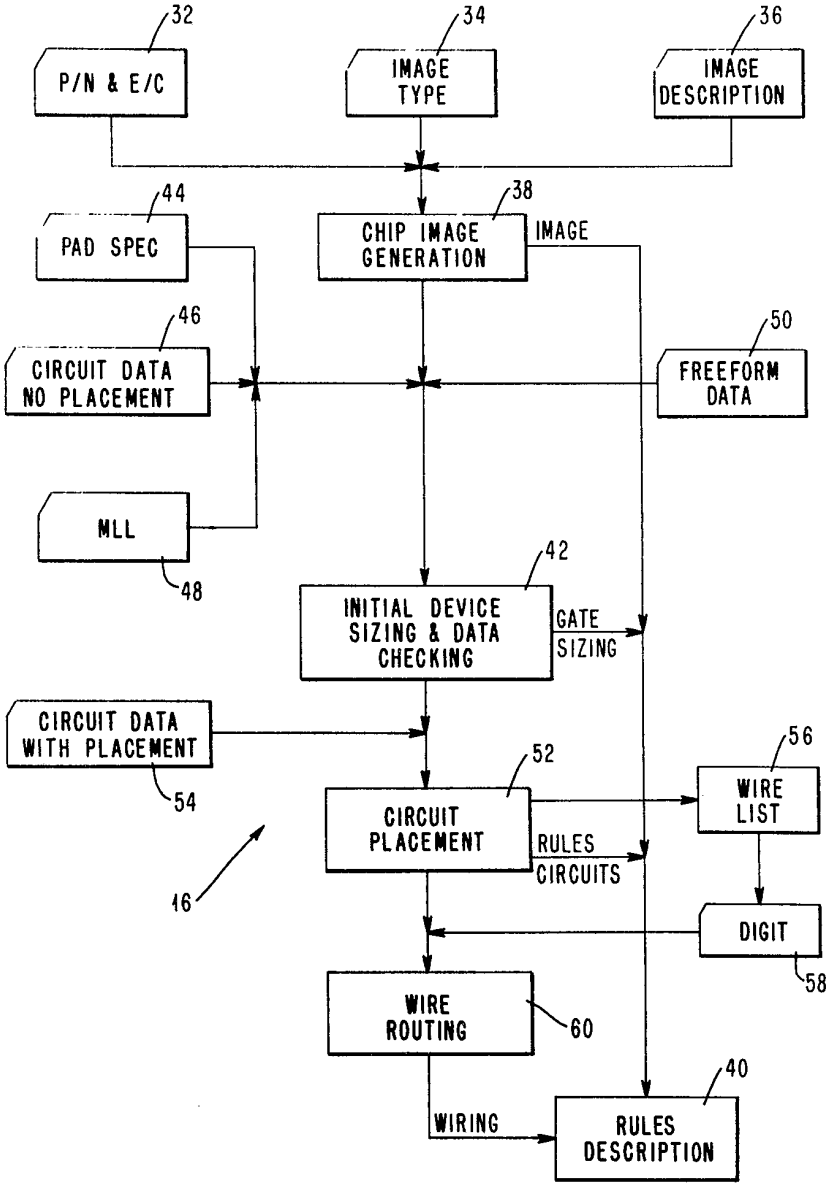
Sheet 3

FIG. 4



1445914 COMPLETE SPECIFICATION
6 SHEETS *This drawing is a reproduction of the Original on a reduced scale*
Sheet 4

FIG. 5a

46 (54)

CIRCUIT NUMBER	BOOK NUMBER	COLUMN	ROW	ORDER	ORIENTATION	LOAD DEVICE	LOAD WIDTH	FUNCTION	SUB-FUNCTION	SPECIFICATION	SPECIFIED LST	DELAY LST
1	1	(1)	(2)	(1)	(1)							

CIRCUIT DATA

FIG. 5b

50

CIRCUIT NUMBER	BOOK NUMBER	X LOCATION	Y LOCATION	ORIENTATION
2	401	10	50	1

FREEFORM DATA

FIG. 5c

48

NET NUMBER	CIRCUIT NUMBER	LST ID	CIRCUIT	LST ID	CIRCUIT	LST ID
101	2	B01	-1	P41		
102	2	Z02	1	A01		
103	1	Z01	-101	P36		

MASTER LOGIC LIST (MLL)

1445914 COMPLETE SPECIFICATION
6 SHEETS *This drawing is a reproduction of the Original on a reduced scale*
Sheet 5

FIG. 5d

44

LOGICAL I/O	PHYSICAL I/O	WAVEFORM	RISE TIME	FALL TIME	CAPACITANCE
P41	P41		100	200	
P36	P36				5

PAD DATA

FIG. 5e

58

NET NUMBER	CODE	X START	Y START	Z START	WIDTH	DIRECTION	STEPS
101	1	a	b	c	o		
102	1	d	e	f	o		
103	1	s	n	i	o		

DIGIT DATA

FIG. 5f

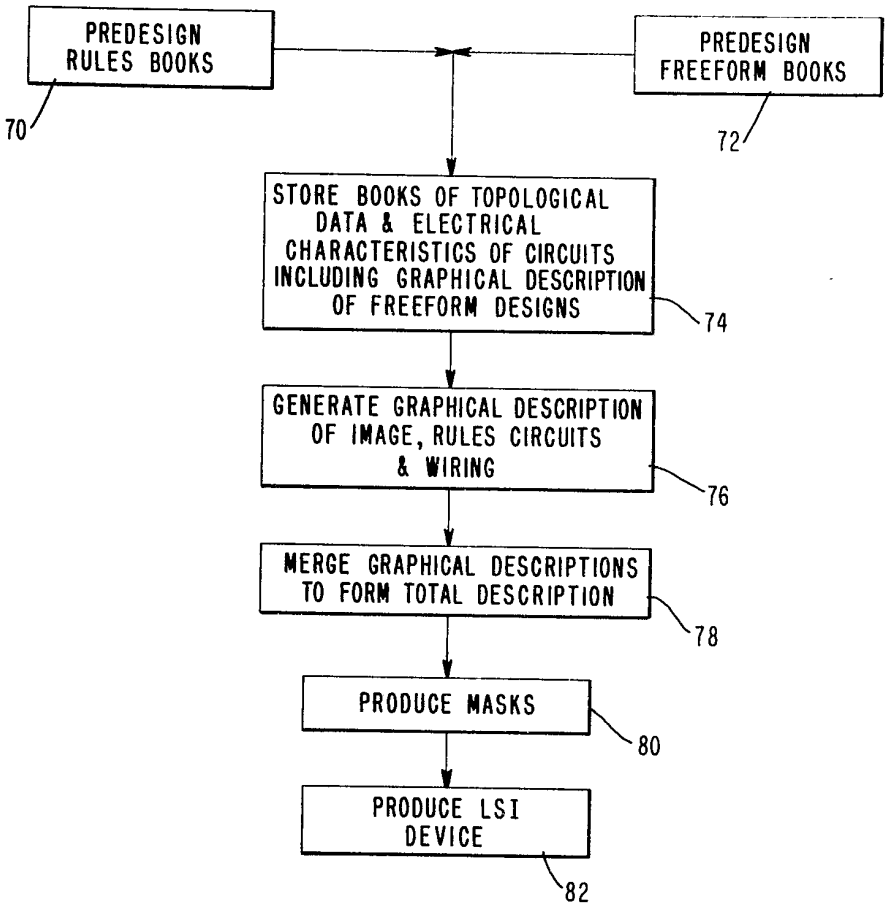
34

DEFAULT IMAGE	COLUMNS = N

IMAGE TYPE

1445914 COMPLETE SPECIFICATION
6 SHEETS *This drawing is a reproduction of the Original on a reduced scale*
Sheet 6

FIG. 6



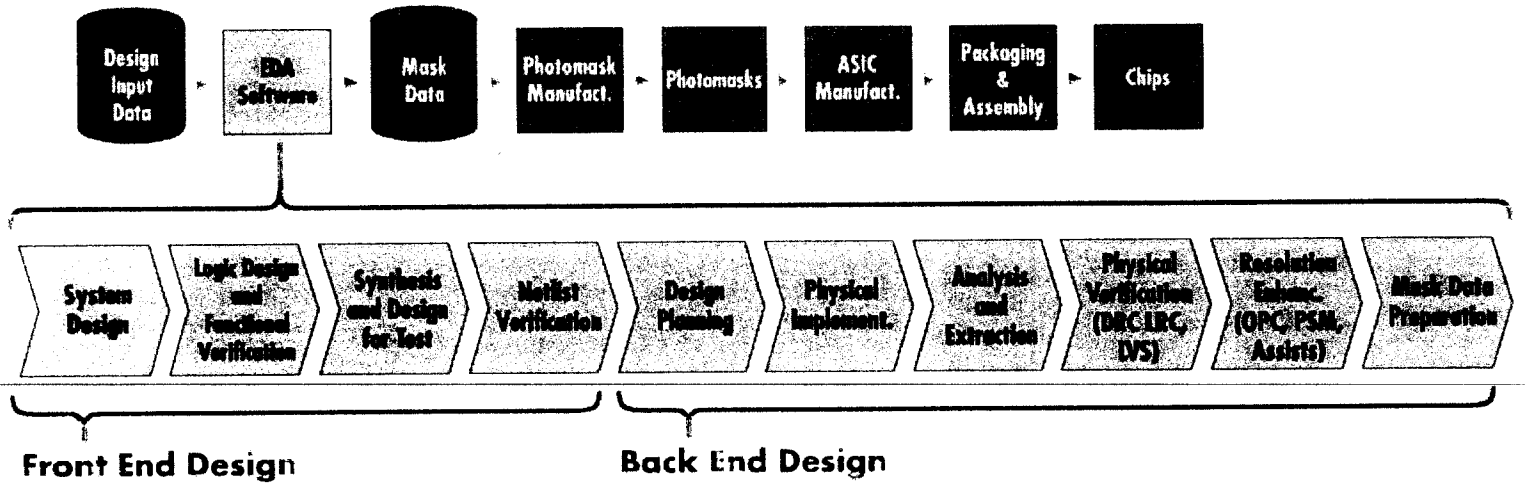
Claim 13

PREAMBLE/TERM 8

13. A computer-aided design process for designing an application specific integrated circuit which will perform a desired function comprising

'432 Patent 16:34-36

- **Dispute: Ricoh seeks to add "during the manufacture" to Claim 13**
  - **Avoid dismissal for use by foreign defendants (35 U.S.C. §271(g))**
  - **Attempt to enlarge measure of damages based on chips**



Demystifying Chipmaking

by Richard F. Yanda, Michael Heynes and Anne K. Miller

ELSEVIER

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Foreword

Welcome! This is the story of how the vast majority of integrated circuits are made—call them "computer chips," if you like, although a host of other electronic components are made in much the same way. Everyone who is curious about how such tiny, yet powerful, devices are made will enjoy the story. This book will also serve as a valuable update to those who may be unaware of how drastically the state-of-the-art processes have changed in recent years.

The most glamorous (and expensive) part of the chipmaking process is the focus of this book. A chip will be built: each step is described, in order, until the whole chip is completed, from the design phase, to growing the silicon ingots, to the final testing of the packaged part.

The building of a chip is a fascinating process that will certainly impress and astonish everyone who is new to the story or who is out of touch with current procedures. Read on!

***Definition**: Tapeout* is the process of turning the layout (chip artwork) into separate layers that will be made into photomasks (see Section 5). The term comes from the procedure used early in the history of the industry when the final step in the design process was to download the layers onto reel-to-reel tapes. The tapes would then be delivered to the mask maker. Today, tapeout essentially consists of sending an encrypted file of the fully verified IC using file transfer protocol (FTP) to the mask vendor.

only a small portion of the wafer. Multiple exposures are required to transfer the pattern to the entire wafer. These tools have replaced those using photomasks because the image on the reticle can be optically reduced, producing a smaller sized image.

***Definition**: The Quartz Glass* discussed here is fused silica, a high purity form of silicon dioxide (SiO_2).

The reticle is made by patterning a chrome-coated substrate of quartz glass plate. The glass must be defect-free, extremely flat and highly polished. But, more important, it must be transparent to the ultraviolet light wavelengths used to expose the photoresist. All of these requirements are well satisfied by quartz glass.

A thin layer of chromium coats the plate on one side. A glue layer is often needed to ensure that the chrome sticks to the glass and an antireflective coating is needed on top. The total thickness of these films is only about 100 nm.

5.3 Pattern Transfer

***Definition**: Photoresist (Resist)* is a light-sensitive or e-beam sensitive plastic material. Its function is similar to that of the film in a camera, a likeness that will become clear in the next few paragraphs.

The chrome is coated with a thin layer of photoresist. The resist is sensitive to exposure to either an electron beam or a laser. Most ultra large scale integration (ULSI) reticles are produced using an electron beam in a direct-write electron beam system.

Now it is time to utilize the digital code provided by the design group. That code is loaded into the computer that controls the direct-write tool. The layout artwork is reproduced in the resist by the tool, the e-beam is scanned back-and-forth across the resist and the platen on which the glass plate is mounted moves up and down. This intricate control scheme transfers the image into the resist. Exposure to the e-beam or laser energy causes a chemical change in the photoresist.

The pattern is invisible immediately after exposure to the e-beam. A developer solution is needed to dissolve the exposed resist, leaving behind the desired pattern in the resist. Now the chrome is covered with a template that will allow the pattern to be transferred to it.

The next step is to etch the pattern into the chrome. An acid is used that does not attack the resist but easily removes the exposed chrome. A thorough rinse is required after etch, followed by a photoresist strip process to remove the template. The reticle is now complete.

IN THE UNITED STATES DISTRICT COURT
NORTHERN DISTRICT OF CALIFORNIA
SAN FRANCISCO DIVISION
--oOo--

RICOH COMPANY, LTD.,
Plaintiff,
vs.
AEROFLEX, et al.,
Defendant.

No. C03-04669 MJJ (EMC)

SYNOPSYS, INC.,
Plaintiff,
vs.
RICOH COMPANY, LTD.,
Defendant.

No. C03-2289 MJJ (EMC)

TRAVEL TRANSCRIPT

DEPOSITION OF

MICHAEL S. HEYNES

JULY 27, 2005

REPORTER: JUDIE A. NICHOLAS, CSR 12229 JOB 1-2271

IN THE UNITED STATES DISTRICT COURT
NORTHERN DISTRICT OF CALIFORNIA
SAN FRANCISCO DIVISION
--oOo--

RICOH COMPANY, LTD.,)
)
Plaintiff,)
)
vs.) No. C03-04669 MJJ (EMC)
)
AEROFLEX, et al.,)
)
Defendant.)
)

--oOo--

BE IT REMEMBERED that, pursuant to Notice, and on Tuesday, July 27, 2005, commencing at 10:19 a.m. thereof, at 177 Post Street, San Francisco, CA, before me, JUDIE A. NICHOLAS, a Certified Shorthand Reporter, personally appeared

MICHAEL S. HEYNES,

called as a witness by the Plaintiff, who, having been first duly sworn, was examined and testified as follows:

DICKSTEIN SHAPIRO MORIN & OSHINSKY, 2101 L Street NW, Washington DC 20037-1526, represented by Eric Oliver, Attorney at Law, appeared as counsel on behalf of the Plaintiff.

Howrey, 525 Market Street, Suite 3600, San

Francisco, CA 94105-2708, represented by Jaclyn C. Fink, Attorney at Law, appeared as counsel on behalf of the Defendant.

--oOo--

EXAMINATION BY MR. OLIVER

MR. OLIVER: Q. Good morning, Mr. Heynes.

A. Good morning.

Q. Would you please state your name, your full name, and your address for the record?

A. Michael S. Heynes, 1501 West Hillsdale Boulevard, No. 111, in San Mateo, California 94402.

(Exhibit 50 marked for identification.)

Q. I've set before you what has been marked as Plaintiff's Exhibit 50. Do you recognize that?

A. Yes.

Q. What is that?

A. This is an e-mail that I sent to Jackie Fink after the first conversation I had with her, and it was just a couple of my thoughts concerning the ASIC -- the structure of the ASIC integrated circuit market.

Q. If you could just speak up a little bit louder.

A. Oh, okay.

Q. Says here, "After our conversation yesterday," which would have been June 6th, 2005, "I was thinking about ASICs."

What was your conversation?

MS. FINK: Objection to the extent that it calls for privileged information.

MR. OLIVER: Just to clarify, is he not an expert, designated as an expert?

MS. FINK: Yes.

MR. OLIVER: So you're claiming that there's some type of privilege in connection with this --

MS. FINK: It could be work product.

MR. OLIVER: Or work product?

MS. FINK: (Nodded affirmatively.)

MR. OLIVER: Just to be clear, were you representing him at that time, June 6th?

MS. FINK: We had -- actually, at that point, we hadn't yet signed a retention letter.

MR. OLIVER: Either way, you weren't representing him --

MS. FINK: No.

MR. OLIVER: -- in a legal capacity, so, just to be clear, any conversation you had with him on June 6th could not have been a privileged conversation.

MS. FINK: Okay.

MR. OLIVER: Q. Do you remember the question?

A. You were asking the nature of our conversation.

Q. Yes.

A. And I don't remember much about it. It was a very -- it was our first phone conversation, and it was a very general conversation.

Q. Did you initiate the conversation?

A. Jackie called me.

Q. Do you know why she called you?

A. She was looking for someone with expertise in the integrated circuit fabrication area.

Q. Just the fabrication area?

A. Yes.

Q. Do you know how she found you?

A. It was a referral from someone else that she had called before.

Q. Do you know the name of the person who referred you?

A. Yes. I was referred by Ann Miller of a company called Semiconductor Services, which is a small training and consulting company.

Q. Do you know if she contacted anyone else after she contacted you?

MS. FINK: Objection. Calls for speculation.

THE WITNESS: I'm sorry.

MR. OLIVER: Q. You can answer if you know.

A. Not that I know.

Q. When were you retained to be an expert in this

Page 6

case?
A. That was the -- I think probably the day after this conversation, and Jackie sent me a letter of agreement for me to sign.
Q. The day after the June 6th conversation?
A. I think so.
Q. Were you retained solely for the preparation of the declaration that you signed and was filed -- or at least was signed on June 14th, 2005?
A. I don't know that that's all that Jackie had in mind for me.
Q. Have you done anything else for -- I guess Synopsis is the person who actually retained you, is that correct, as opposed to Jackie's law firm?
A. Indirectly.
Q. So you worked for Howrey, but Synopsis is the ultimate --
A. Yes. Yes.
Q. Okay. Well, have you done anything else besides your work on the declaration?
A. No.
Q. Is there anything else -- any future plans to use you, that you know of?
A. Not that I know of.
Q. In the third paragraph you use the phrase,

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"Another approach is to fab wafers with a standard chip design." What are you referring to in that paragraph?
A. This is a technology which is used where standard wafers are processed up to the metallization level, and those wafers will have the whole range of different kinds of cells and devices on them, and they can be wired together to produce essentially an infinite number of different functions. And at the time that I wrote this e-mail, I didn't know very much at all about the nature of this particular case, and apparently the ASICs involved here are not of these gate array types, but a complete custom design, basically. ASICs used to be called custom design.
Q. You have attached a CV which appears as the second and third pages of this exhibit. Is that the same CV that was attached to your declaration?
A. Yes.
Q. You mention calling Katie Yanda. Who is Katie Yanda?
A. She's the wife of a man who is one of the three authors of the book that's referred to in the declaration.
Q. She was the wife of --
A. Of Richard Yanda, actually -- Richard F. Yanda, who is one of the three authors of the book that's

Page 8

mentioned, and she has worked in the industry for a long time, in the design area.
Q. Was she also an author of that book?
A. No.
Q. Why did you call her?
A. I called her to let her know that she may get a call from Jackie.
Q. Did you refer her to Jackie?
A. Yes.
Q. Why did you refer her?
A. Because she was someone I knew who was very familiar with the design activity.
Q. As opposed to the fabrication process?
A. Fabrication activity, right.
Q. Has she written her own books?
A. No. Not to my knowledge.
Q. Turning to the second and third pages of the document -- or of the Exhibit 50, I'd like to step through your work experience.
Currently you work as a consultant, is that correct?
A. Yes.
Q. Do you do any consulting work for Synopsis?
A. No.
Q. Do you any work -- consulting work for any of

Page 9

the ASIC defendants in this case, which are Aeroflex, Matrox and AMIS?
A. No.
Q. You know who all those companies are, is that correct?
A. Vaguely, yes. Not well.
Q. Have you ever worked for any of those companies?
A. No. Who was the last one you mentioned?
Q. AMI Semiconductor?
A. Oh, I have worked for AMI Semiconductor twenty years ago.
Q. Is that what you have down as -- let's see if it's on here.
A. Yes, that would be in the previous position section. Manager, CMOS Technology Development, American Microsystems.
Q. Yes, American Microsystems. We'll get to that in a minute.
As a consultant, what are your duties?
A. Mostly, in recent times, it's been training. I've written many training classes and presented them to a variety of different audiences, from equipment companies particularly, and sometimes to semiconductor companies, chip-making companies.

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Q. And what aspect -- I assume this involves semiconductor of processing?
A. Yes.
Q. Manufacturing processing?
A. Yes. Sometimes overall wafer fabrication, sometimes relatively specialized material. I've done a lot of work for Lam Research, one of the major equipment company makers, on etch processes for etching the patterns on silicon wafers, and so those classes were focused on the use of Lam's equipment in wafer fabrication.
Q. So you don't do any design or engineering consultation, is that correct?
MS. FINK: Objection.
THE WITNESS: Sorry.
MS. FINK: Lack of foundation. Mischaracterizes his prior testimony.
THE WITNESS: I can answer?
MS. FINK: Yes.
THE WITNESS: Nothing connected with the design. I know very little about design engineering. I'm a process engineer.
MR. OLIVER: Q. Have you ever had any duties in any job capacity with respect to designing of integrated circuits?

Page 11

A. No.
Q. With designing of any type of circuits?
A. No.
Q. You were with Lam Research?
A. Yes, I was with Lam Research as an employee for a few years, and then continued on a consulting basis with them.
Q. What did you do at Lam Research?
A. That was all training. They wanted someone who had experience in the overall wafer fabrication area, because the people who work in the equipment business generally don't understand well how their equipment is used in fabricating wafers.
Q. What is their equipment?
A. Their principal product is plasma etchers.
Q. And what does one do with plasma etching?
A. They etch -- those machines can etch many kinds of materials to form the patterns in the surface of the silicon wafers.
Q. And they didn't understand how that fed into the overall process, is that what you're saying?
A. Yes.
Q. Did you do anything else there?
A. No.
Q. When you were with -- prior to that you were with Teledyne Components?
A. Yes.
Q. What did you do there?
A. That was a small division of Teledyne Corporation, which has a number of divisions in the various technology areas, and they made small volumes of specialized chips. And, again, my responsibility there was in wafer fabrication.
Q. What, in particular, did you do?
A. I was doing improvement of an existing CMOS technology wafer fabrication process. That took a lot of time.
Q. When you say you worked on an improvement, exactly what was your responsibility?
A. The wafers that they were fabricating were yielding rather poorly, not many good chips per wafer, in other words, and I was looking at wafers to try to find out why they had these yield problems, and, also, looking at the various process steps through the fabrication cycle, I was looking for places where I could improve what are called individual process modules, where perhaps the thicknesses or other characteristics of the materials were not as well controlled as they should be.
Q. So if you found an area which could be improved, what did you do?
A. I would do a number of experiments on that particular process to establish a new way of running that process, and write a specification for it, and train technicians and operators to run the process and follow the specification.
Q. In the previous position section, you worked for Gain Electronics.
A. Uh-huh.
Q. When did you work for Gain Electronics?
A. That would have been about 1988 to 1990.
Q. And what did you do at Gain Electronics?
A. This was a very different technology, because I was working with gallium arsenide.
Q. So what did you do there?
A. The nature of the work I was doing was similar to my silicon experience. I was working on etching patterns, I was working on chemical vapor deposition processes for the deposition of things like silicon nitride layers. Those are two principal areas where I worked. This was a small startup company and just getting wafer fabrication going.
Q. Were you again responsible for determining why yields were low?
A. At the point I was working there, it was a new

Page 14

company. They were not yet making circuits at all. They were developing a process, a technology.

Q. Were you in charge of that process?

A. Not in that case, not the whole process. The way I have been -- with silicon in several companies, I had these rather specialized, relatively individual contributor responsibilities for those certain process steps, like the chemical vapor deposition and etching processes and plasma-activated machines.

Q. So when you say you worked in those aspects, what did you actually do?

A. Taking test wafers, and in some cases just bare wafers, putting them in a chemical vapor deposition machine, depositing layers of silicon nitride on them and then evaluating those layers with uniformity across the wafers, the optical characteristics of the wafer's refractive index notably, which is an indication of the structure of the silicon nitride material.

Q. Then you were with American Microsystems, is that also known as AMI?

A. This is going back in time. Before -- AMI was before Gain Electronics.

Q. I'm sorry. Yes.

So, American Microsystems, that's also known as AMI, is that correct?

Page 15

A. Yes.

Q. And when did you work there?

A. Roughly, from 1990 to 1995.

Q. And what did you do at AMI?

A. That's where I was responsible for -- most of the time I was there -- for an overall wafer fabrication technology development. The company already had a CMOS technology which was outdated, and my principal task was to develop a next generation CMOS fabrication cycle is a way of expressing it.

Q. Did you deal in any way with the design phase?

A. No.

Q. Did you interact with any design engineers?

A. A little.

Q. When you say a little, what do you mean?

A. I was -- the responsibility I would have would be in taking masks for a CMOS process and running them through our new CMOS wafer fabrication cycle, and the design engineers would be interested to know when are the wafers coming out.

Q. So your interaction involved reporting to them?

A. Keeping them informed past the progress of wafers which were in fabrication and passing them on for a test.

Q. Since 1985, have you ever had any interaction

Page 16

with AMI or anyone in AMI?

A. No. I had one person from AMI in a class at Lam on one occasion, a man I never met before. He was a young man I never met. That's the only contact I've had with AMI since.

Q. Have you ever had any contact with anyone from Aeroflex?

A. No. No.

Q. Have you had any contact with anyone from either Matrox Electronic Systems, Matrox Graphics, Matrox International Corp. or Matrox Tech?

A. No, I had never heard of them.

Q. In forming your opinions for your declaration, did you do any analysis of any design work, or any work whatsoever from any of the ASIC defendants, those being Aeroflex, Matrox, or AMI?

A. No. No. I have no knowledge in that area to do such work.

Q. Why did you refer Katie Yanda to Jackie?

A. She was someone I knew who had worked in the design area for a long time.

Q. Yes. But I meant did Jackie express an interest in finding someone who had design experience?

A. Yes, she had asked me if I could refer her to someone who had that background.

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Q. Do you know if Jackie or anyone at Jackie's law firm had contacted Katie Yanda?

A. No.

Q. When did you work at Microtechnology?

A. That would have been before --

Q. Do you have an approximate time?

A. That would be about '78 to '80.

Q. And what did you do at Microtechnology?

A. Again, I was running wafers through a CMOS fabrication process.

Q. What did you do at Nortec Electronics?

A. I was doing some process development, the kind that I described for Gain Electronics, individual process modules which needed developing from scratch or needed improving, and also putting together complete process runsheets as they call it, the complete cycle of steps that wafers need to go through in wafer fabrication. It's called process integration.

Q. And what year was -- what year did you work at Nortec Electronics?

A. That went from about 1970 to 1978.

Q. Is it safe to say you did similar work involving fabrication processing for the companies listed in your early work section?

A. Yes.

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Q. Is there any other companies that you may have worked for that are not listed anywhere on this CV?
A. My very first job in the U.S -- I completed my education in England. My first job in the U.S. was with a company called Clevite.
Q. How do you spell that?
A. C-l-e-v-i-t-e. In the Boston area.
Q. When did you work there?
A. I came to the U.S. in 1960 and worked there until about '64.
Q. Did you work also in the fabrication process?
A. Yes. Actually, my first job there was in crystal growing. My first responsibility was growing crystals, silicon crystals, and doing a process called epitaxial deposition. It's a technique for putting a layer of silicon on an existing silicon wafer.
Q. How many books have you written, or co-authored?
A. That's the only book of a textbook style. I have a number of publications in the academic literature, maybe seven or eight articles in the academic literature on semiconductor processing diffusion, some chemical vapor deposition, some MRS technology and related material.
Q. Did you author a book called Semiconductor

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Technology, Glossary of Terms?
A. No, I didn't. I wrote an article for a magazine which may have had that title, come to think of it, but there's hundreds of those glossaries around, and I've written several of them for several jobs.
Q. I see. So it may not have been a book, it may have been just a publication?
A. Yes, that was an article in some electronics magazine.
Q. And was that with Ann Miller?
A. No. No, that was way -- a long time ago.
Actually, there was one article more recently which was -- that was not a glossary, that was more of a general -- very general outline of MRS technology.
I was at Nortec when I wrote that glossary article, so that goes back to the seventies.
Q. Did you write that yourself?
A. Yes.
Q. Did you write a book entitled Integrated Circuit Manufacturing Synopsis?
A. I helped write some sections of it. It's a small -- very small book, a dozen pages or something like that. It's a very broad outline of the whole of the semiconductor industry, essentially.
Q. What the book about?

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A. It's a very high level view of the whole semiconductor industry, of semiconductor chip fabrication.
Q. Was Ann Miller a co-author?
A. Yes.
Q. What was your role in writing the book?
A. Actually, it was an updating activity which I participated in. She already had this synopsis written and was using it, and it needed updating because of changes in the process technologies.
Q. So you worked on the updating of the book?
A. Yes.
Q. So I presume you read it and you found it to be accurate, is that correct?
A. I must have.
Q. Do you know of anything that was incorrect?
A. I may have -- certainly not that I remember now. I may have disagreed with Ann at some point, and she may not have -- she was -- it was her book to publish and I was helping her to put it together.
Q. I see.
A. I may have disagreed with her on some points, and she may or may not have taken my suggestions.
Q. As to the Demystifying Chip Making book, that was -- you were the principal of that book? That's

Page 21

correct?
A. Yes. I'm not the first mentioned author. I should explain that. Rick Yanda likes to write, I don't, so I was main the source of information for most of the material in the book and he put the words together.
Q. I see.
A. I --
Q. So that's why you, on your CV, call yourself a principal contributor?
A. Yes.
Q. So it's really, you believe, your work?
A. Yes. I wrote many sections and gave those drafts to Rick, and this is intended to be an introductory book, and my writing style is rather terse and academic, so Rick modified it to make it easier for the less educated people to read.
Q. So you're pointing to Jackie when you say that?
A. Jackie said it was very clear.
Q. I see.
A. So Rick did the write thing with my terse academic stuff.
Q. So you found that book to be accurate, is that true?
A. In the areas where I have expertise, with one

Page 22

exception. There was something I disagreed with Rick Yanda on which I wanted to change, at least one thing that I know of, and he chose not to change it.

Q. What is that?

A. This had to do with a P-N junction, and the electrical charges in it. This is device physics.

Q. So you disagreed with that and he did not change it?

A. Right.

Q. Was there anything else that you disagreed with?

A. Not that I remember.

Q. Now, this Rick that we've been talking about is Richard Yanda?

A. Yanda.

Q. Husband of Katie Yanda?

A. Yes.

Q. Who is Richard Yanda?

A. He's worked the industry for, I suppose, 20 years or something like that. Yeah, probably about 20 years.

Q. Would you consider him an expert in the field?

A. He's an expert in a relative limited area. He is more expert, for example, in plasma etching than I am, because he had spent many years at Lam in field

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engineering, helping customers fix their problems.

Q. Would you say he has experience in the manufacturing of integrated circuits?

A. Yes, he's worked in fabrication. At Lam he was not working in a wafer fabrication operation, since Lam was an equipment builder, but, in the course of his job, he would be working inside fabs of various chip-making companies, and he had also worked, in a more general sense, in the chip making company. Enmass was one company. And maybe Cypress, I'm not sure.

Q. Do you know if he has had any experience in the design phase of chip making?

A. I don't know. I don't think so.

Q. And we spoke about Ann Miller previously. Who was Ann Miller?

A. Ann is a woman who worked in the industry for a number of years, and then she had worked for companies like KLA, and she hadn't been an employee of Intel but she had been assigned there by her company which was making materials for lithography, but she bought a training company called Semiconductor Services from Peter Van Sant, who is a well known book writer, an introductory book on wafer fabrication.

Q. What was her experience in the industry?

A. The years that she had spent working at Intel,

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as I say, on assignment from a company that was a company, a chemical supplier, and her years at KLA, which was an equipment company.

Q. I have this title of a book it's called Semiconductor Terminology, Graphic Glossary of Terms, by Michael Heynes, PhD, and Ann Miller, Fourth Edition, 2002, 45 dollars.

Is that your book or publication?

A. Yes. She had a -- I'd forgotten that glossary was part of the title there. That's the one that you were talking about earlier.

Q. Yes.

A. I didn't recognize the glossary was in the title of that. I haven't looked at it for at least two years.

She had a book of that name which she and other collaborators had put together. I found many technical errors in it, and worked collaborating with her on a major updating.

Q. And so the 2002 edition, or version, is the current edition?

A. Yes.

Q. And you believe that is now accurate? You've corrected the errors that you felt were there, is that correct?

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MS. FINK: Objection. Misstates his prior testimony.

THE WITNESS: Again, I made suggestions, in some cases which perhaps Ann did not necessarily follow in the final draft.

(Exhibit 51 marked for identification.)

MR. OLIVER: Q. I've put before you what has been marked as Plaintiff's Exhibit 51, which is a Notice of Subpoena for your deposition. Have you seen this document before?

A. Yes.

Q. Who gave you this document?

A. Jackie sent it to me about the end of last week.

Q. Did she tell you that you would be required to produce documents as listed in the subpoena?

A. Yes.

Q. Did you do so?

A. Yes.

Q. Did you have any notes that should have been produced?

A. No.

Q. You didn't make any notes?

A. I actually -- when Jackie and I talked yesterday, you know, Monday, I had made a couple of

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margin notes on one of the documents, and she said I have to take that and give it to you, I guess.
Q. Did you do that?
A. Yes. I gave it to Jackie.
Q. Do you remember which document that was?
A. It was my declaration.
MR. OLIVER: Jackie, I don't remember seeing any handwritten notes in the documents that were produced to me.
MS. FINK: I can look for that and produce it.
MR. OLIVER: This is the copy have that I received. Do you want to take a look at that?
MS. FINK: I think we may have sent these before that, but I can look to see if I have it.
THE WITNESS: Like I said, it wasn't until Monday.
MR. OLIVER: I see. Okay. So you'll --
MS. FINK: I will look.
MR. OLIVER: If we have any other questions, we'll have to somehow work out the details getting answers to them.
Q. Were there any other notes that you had made at any time?
A. No. This is a relatively simple thing to review.

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Q. What you were asked to do?
A. Initially, Jackie sent me a copy of the patent and the construction, and I reviewed those documents. Those were the principal documents that I looked at.
Q. What did she ask you to do with respect to those documents?
A. To look through the patent and see how it related to my expertise.
Q. Did you generate any invoices?
A. Yes. Yes, I generated one invoice for the end of June to Synopsis.
Q. Did you include that in the material that was to be produced?
A. No.
Q. Let's take a look at the list, just to be complete. In this Exhibit 51, attached to the subpoena there's a Request For Production on page 6.
A. Since that was not a technical document, I didn't think of it.
Q. This is page six. I don't know how far into the document it is.
Request number one with is all documents and things received from or provided to or on behalf of the defendants, Howrey, and Synopsis related to your declaration.

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Did you produce those items?
A. I believe so, with that exception.
Q. That exception being what?
A. The invoice.
Q. I believe that's in another category, but that certainly also falls in that first one.
All communications, that's Production Request Number 2. Did you produce all communications?
A. Yes. Yes. There's the file which you were looking at there.
Q. Production Request Number 3, it's all documents you reviewed, analyzed and considered in connection with your declaration. Other than the patent and the claim construction, did you consider anything else?
A. No, I don't think so.
Q. Did you read any textbooks in connection with the declaration?
A. No.
Q. Did you consult with anyone?
A. No.
Q. Did you talk with anyone whatsoever?
A. Not that I recall.
Q. Did you talk with any -- with Jackie or any other attorneys when preparing your declaration?
A. Yes.

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Q. Okay. Who did you speak with?
A. With Jackie.
Q. Just Jackie?
A. Yes.
Q. And Request Number 4 asks for draft notes, memoranda, worksheets, calculations, e-mails, faxes, phone messages, correspondence and invoices. With the exception of invoices, did you --
A. It was there, wasn't it?
Q. Did you produce everything, other than the invoices?
A. Yes. Yes.
Q. How much time did you spend in preparing the declaration?
A. Most of that time was spent with Jackie. It was approximately four hours. Maybe an hour in preparation before -- reviewing the documents before I came in to see Jackie.
Q. All things related to preparation, creation, drafting, revision and/or finalization of the declaration is Request Number 5. Did you go through many drafts of the declaration?
A. With Jackie, we worked through the draft, and I called for quite a lot of modifications as we went through it.

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Q. Who did the first draft?
A. Jackie had a kind of outline based on her research work on wafer fabrication and put together a general outline of what wafer fabrication was about, and then I worked with her to modify it and bring it to the point where I agreed with everything that was there.
Q. So she had done research on wafer fabrication?
A. Yes. Yes. She had read the book.
Q. The book being --
A. She had been reading the book Chip Making Demystified.
Q. And the last request is all things related to the 432 patent, the file history, and any art cited. Did you review the file history of the 432 patent?
A. No.
Q. Did you review any art cited in the prosecution of the 432 patent?
A. No. The patent is all design software where I have very little understanding.
Q. You have what type of understanding?
A. I have little understanding of the software of the design activity.
Q. Does that mean you have little understanding of the patent?

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MS. FINK: Objection. Misstates his prior testimony.
THE WITNESS: I understand the overview of what the patent is about. I understand the general statements it makes on the purpose of the software and what the end result is of the software.
Q. As far as the details --
A. The details of how the software is put together and the jargon and -- the software jargon which is in the patent -- is outside my area of expertise.
Q. Did you read the claims of the patent?
A. Yes.
Q. Which claims did you read?
A. I read all of them.
Q. Did you understand them?
A. Some of them. Some of the general statements I understood. Again, the ones relating to software details I did not understand, or only in the most general way.
Q. Did you remember a Claim 13?
A. Yes, I remember a Claim 13.
Q. Let me give you what has been previously marked as Kobayashi Exhibit 9. And if you can turn to the end of the patent, there's a Claim 13 in Column 16. Do you see that?

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A. Yes.
Q. Do you recall reviewing that claim?
A. Yes.
Q. Did you understand that claim?
A. In a rough way, yes. Not in detail because, again, this is all about software.
Q. What did you mean, in a rough way?
A. Well, the initial -- "A computer-aided design process for designing an application specific integrated circuit which will perform the desired function, comprising." I certainly understand that sentence, and I understand what storing data consists of, but I'm not quite sure what -- an expert system knowledge basis, that's software jargon, and so on, so -- I understand, as I say, in general what it is about, but the software aspect of it I don't understand very much of.
Q. Did you review Claim 14?
A. Yes.
Q. Did you understand Claim 14?
A. Yes.
Q. What is your understanding of Claim 14?
A. It's a process which has been described in the previous claim for generating from the netlist the mask data, the next step from the netlist, generating the mask data which is required to produce actually masks,

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not integrated circuits.
Q. What did you mean by that?
MS. FINK: Objection. Vague and ambiguous.
MR. OLIVER: Q. The last part where you said mask data, which is required to produce masks, not integrated circuits, what did you mean when you say that?
A. Mask data alone does not enable you to produce an integrated circuit.
Q. Why is that?
A. Because to make an integrated circuit, you need masks.
Q. True, but the claim just says mask data required to produce an integrated circuit. In other words, before you can produce an integrated circuit, you need mask data, is that correct?
A. Yes.
Q. I'm going to give you what has been marked as Plaintiff's Exhibit 52. Have you seen what is Exhibit 52 before?
A. Yes.
Q. What is it?
A. This is my declaration.
Q. It's the declaration you were talking about previously.

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Previously you had testified that, in preparing this declaration, Jackie had an outline for you, is that correct?
A. Yes.
Q. Did you yourself write most of the text in this declaration?
A. Much of what Jackie had written was acceptable to me, but I made many modifications. I did not do the original writing of the outline. Obviously, Jackie did that.
Q. When you say outline, you mean she had given you a first draft of the declaration?
MS. FINK: Objection. Asked and answered.
THE WITNESS: She had put together an outline based upon what she had learned from her research and reading the book and other sources.
MR. OLIVER: Q. When you say outline and then you describe what she did, it sounds like she did a first draft in detail.
A. She had some detail --
Q. An outline to me is just bullet points. Is it safe to say she did more than just a bullet point outline?
A. Yes. There was some paragraph writing, but a lot of bullet points, which we modified, expanded, when

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we worked together.
Q. Did Jackie explain to you what this declaration would be used for?
A. Yes.
Q. What did she explain to you?
A. I don't recall in detail.
Q. What do you recall?
A. I don't think she explained, actually, in a lot of detail. It was a document which was to express the way that I saw the industry working. My work experience is what I've relied on in reviewing this material and working with this material, the way I have seen the industry work.
Q. Did she tell you what the purpose of the declaration was?
A. I don't think I can define that.
Q. Did she tell you it dealt with chip manufacturing?
A. Oh, yes, of course.
Q. Did she tell you anything in particular about chip manufacturing that you needed to describe in the declaration?
A. Would you rephrase that?
Q. Did she tell you what aspects of chip manufacturing she wanted to have you describe in the

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declaration?
A. Yes. She wanted me to cover, essentially, the whole of wafer fabrication.
Q. All of your experience has been -- in terms of wafer fabrication, is that true?
MS. FINK: I'll object. Vague and ambiguous. As contrasted to what?
MR. OLIVER: Q. Previously -- let me clarify. Previously we discussed your work experience.
A. Yes.
Q. And you detailed all of your work --
A. Yes.
Q. -- in terms of wafer fabrication, is that correct?
A. Yes. I was trying to think if there were any exceptions to that. That's why I paused. I think that is true, it has all been wafer fabrication.
Q. In your mind, manufacturing of ASICs or ICs in general starts with wafer fabrication, is that true?
A. Yes.
Q. So you've never used any design tools, is that correct?
A. Correct.
Q. You've never used Design Compiler?
A. No.

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Q. You've never created any circuit schematics?
A. No.
Q. You've never used RTL or VHDL?
A. No.
Q. But you are familiar with some of the terms, is that correct, such as netlist and mask data.
MS. FINK: Objection. Compound.
THE WITNESS: Actually, I -- mask data is -- I didn't know what a netlist was until I read the patent, actually. I knew when I read through the definition of what it was, I said, oh, that's what it's called.
MR. OLIVER: Q. So what is your understanding of the term "netlist"?
A. Netlist is a list of the cells required for a given integrated circuit and information on how those cells are to be wired together to produce the required final function.
Q. Was -- where did you get this understanding of the term?
A. From the patent.
Q. Did you get --
A. It's defined in the patent.
Q. Is there any other source that provided you with any information to inform you with respect to this --

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A. No.
Q. -- definition?
A. No.
Q. Did Jackie give you any input?
A. No. I had heard that term before and just didn't know what it was until I saw it defined here.
Q. Would you be able to step through the manufacturing process, beginning with the initial design of an IC, all the way through to the final packaging?
A. Well, design is not manufacturing.
Q. Well --
A. Design is part of development. It's not manufacturing.
Q. Well, would you be able to summarize for us the steps along the way from design through final packaging of an IC?
MS. FINK: Objection. Exceeds the scope of his declaration. He didn't declare as to --
THE WITNESS: Yes. I don't have the expertise to go through the design cycle and present that. Certainly, I can do it through wafer fabrication for complex processes like CMOS.
MR. OLIVER: Q. But you understand there is a design phase --
A. Yes.

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Q. -- that produces a netlist, as you read in the patent, is that correct?
A. Yes. Yes.
Q. Do you have an understanding what happens to that netlist on its way to manufacturing of an IC?
MS. FINK: Same objection. He didn't opine as to any of the design steps.
THE WITNESS: Only what I read in the patent, that the netlist -- from the netlist, one can make -- produce data for making masks.
MR. OLIVER: Q. Can you say that --
A. From the netlist, you can create data for making masks.
Q. But you're not familiar with that process, is that what you're saying?
A. No. No.
Q. Are you familiar with the term "mask data"?
A. Well, it's self-explanatory. I understand what it means.
Q. What is your understanding?
A. This is electronic information which can be used to make a mask.
Q. What does the mask data represent?
MS. FINK: Objection. Vague and ambiguous as to what you mean by represent.

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MR. OLIVER: Q. Are you able to answer the question?
A. No, I don't know how to answer that question.
Q. Let me ask this. Is mask data a complete representation of the ultimate circuit on the ASIC?
A. No.
MS. FINK: Objection. Vague and ambiguous as to what you mean by complete representation.
THE WITNESS: No. No. It's part of the design phase, and when you talk about a complete integrated circuit, you then talk about wafer fabrication as well.
MR. OLIVER: Q. Can you identify the electronic components in the ultimate ASIC in the same -- in the mask data?
MS. FINK: Same objection. Vague and ambiguous.
THE WITNESS: Not easily.
MR. OLIVER: Q. So mask data is not a layout of --
A. The data is just a bunch of digital information, electronic digital information.
Q. So the mask data does not represent the layout art work, is that right?
MS. FINK: Objection. Mischaracterizes his prior testimony.

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MR. OLIVER: Q. Do you need the question read back?
A. Yeah. Yeah.
MR. OLIVER: Do you mind reading the question back?
(The question was read by the reporter.)
THE WITNESS: From the mask data, you can produce a mask layout.
MR. OLIVER: Q. From the mask data, you can produce --
A. You can produce a mask which shows you the layout.
Q. And what is the layout?
A. The layout is the term we use for the geometry of the patents required on the circuit.
Q. Is the layout a representation of the ultimate ASIC or IC that's being produced?
A. The layout that's produced would be for one patent level to be formed on the wafers. It does not represent a final form in any way.
Q. So are you saying there's multiple layouts?
MS. FINK: Objection. Mischaracterizes his prior testimony.
THE WITNESS: The term is used both for a singular patent and for multiple patents, and different

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people use the term a little differently probably.
MR. OLIVER: Q. What does a layout engineer do?
MS. FINK: Objection. Calls for speculation.
To the extent that you know, you can answer.
THE WITNESS: The layout engineer lays out the expected geometry required for mask levels. I'm not able to define it well.
MR. OLIVER: Q. Does he produce mask data?
A. I don't know if there's another step following that.
Q. Does the layout engineer draw a picture of the actual finished device as seen from the top?
MS. FINK: Objection. Calls for speculation.
THE WITNESS: To some extent. In CAD equipment, computer aided design equipment, there are images on the screen of layouts, of patent geometries.
MR. OLIVER: Q. Are you familiar with the term tape-out?
A. Yes.
Q. What is tape-out?
A. Tape-out is -- it goes back to the days when the electronic data was on big reels of tape, and that tape would be sent to mask makers to make the mask set for it.

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Q. Is the mask data part of the tape-out?
A. The mask data is on the tape.
Q. It is the tape-out, right?
A. It's the tape-out.
Q. What do they do today? You said previously they had these big tapes. Now what do they do?
A. Yes. Actually, today they don't use the tapes anymore, the data is communicated electronically.
Q. To where?
A. To the mask making shop.
Q. So this data -- the mask data is sent or fed to the mask --
A. The shop where the masks are going to be made, which is --
Q. A mask vendor.
A. Yes, a mask vendor, which is usually separate from the design activity and the fabrication activity. It might be on the other side of the world.
Q. So the mask data or the tape-out is fed into some mask vendor.
A. Yes.
Q. Is that correct?
A. Yes.
Q. Is the tape-out the process of turning the layout or chip art work into separate layers that will

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be made into photo masks?
A. Yes.
Q. Did you say wafer fabrication is an essential part of ASIC production?
A. It is ASIC production.
Q. So you would say it's --
A. Design is not production. Making masks --
Q. I didn't ask you anything about that. I said is wafer fabrication an essential part of ASIC production.
MS. FINK: Objection. Asked and answered.
MR. OLIVER: Q. Is that a yes or no?
A. It is ASIC production.
Q. So it's directly related to --
A. It is manufacturing. It is the manufacturing of a part.
Q. Okay, so the wafer fabrication is directly related to the manufacture of an IC, correct?
A. It is the manufacture of an IC.
Q. Is the use of a mask an essential part of ASIC production?
A. Yes, it is.
Q. Is it directly related to the manufacture of an IC?
A. Yes, it is.

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Q. Is the use of mask data an essential part of the ASIC production?
A. It's not part of production.
Q. Why not?
A. It is part of design.
Q. Why?
A. Because mask data does not enable you to make wafers. You don't go directly from mask data to wafers.
Q. Is that the only reason?
A. I'm trying to think if there is -- repeat the question so I know exactly how you worded it.
Q. Is the use of mask data essential to ASIC production?
MS. FINK: I'll object. Vague and ambiguous as to what you mean by essential.
THE WITNESS: No.
MR. OLIVER: Q. So, if you wanted to produce an ASIC, you could do without the use of mask data?
A. No. The mask data is necessary for the production of masks.
Q. I see. And so for an ASIC to be manufactured, you do or you do not need mask data?
A. You need masks, and masks are made from mask data.
Q. From your understanding of the term netlist, do

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you need a netlist to make mask data?
A. Yes, I believe so.
Q. Would you say the use of a netlist is essential in the making of mask data?
A. Repeat that?
Q. Would you say that the use of a netlist is essential to the making of mask data?
A. It may be in this particular package of software. There are other ways of making mask data.
Q. When you say in this particular package of software, what do you mean?
A. The subject of the patent.
Q. And the patent being the 432 patent?
A. Yes.
Q. Would you say that the netlist is essential to the making of a mask?
MS. FINK: Objection. Vague and ambiguous as to what you mean by essential.
THE WITNESS: There are other ways of making a mask besides using a netlist.
MR. OLIVER: Q. What are those ways?
A. A skilled engineer can put together the cells required and devise the wiring without this netlist.
Q. And how do you know that?
A. Because I've been in the industry a long time,

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and this is -- this particular software has not been used.
Q. I thought you said you didn't have any experience in the design phase.
A. I don't.
Q. Is making -- is using a netlist part of the design phase?
A. In -- as far as this particular approach to making a design is concerned, yes.
Q. And so your last question was based on what? If you have no experience in that field, how can you make that statement?
A. Because I know from a long time ago, for example, that design engineers would manually take cells needed for a function and devise a wiring pattern to achieve the function they're looking for. And, to my knowledge, it's very superficial.
Q. Did you know that even when it's done manually, that people would call that collection of cells a netlist?
A. I don't know.
Q. Okay. Let's assume that for the purposes of our -- this next question.
A. Assume that that was called a netlist?
Q. If that is called a netlist, would you say that

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is essential to the making of a mask?
MS. FINK: Objection. Incomplete hypothetical.
THE WITNESS: The assembly of the cells, the choosing of the cells and the wiring of them together, is essential to make the design.
MR. OLIVER: Q. The design of the mask?
A. Yes.
Q. Or the design of the IC?
A. The design of the mask.
MS. FINK: We've going about an hour, can we take a break?
MR. OLIVER: Would you like to take a break?
THE WITNESS: Yeah. Yeah. Stretch a couple of minutes.
(A break was taken.)
MR. OLIVER: Q. Let's try to recreate the question again. We're back on the record.
Would you say that a netlist is essential to the making of mask data?
A. No, because mask data could be made other ways. It could be generated manually.
Q. As we discussed before, if the netlist was generated manually, would you then say that a netlist is essential to the making of mask data?
MS. FINK: Objection. Already asked and

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answered, and lacks foundation. He didn't say that you created netlist data.
THE WITNESS: Repeat the question, please.
MR. OLIVER: Q. Assuming that a netlist could be produced manually, would a netlist be essential to the making of mask data?
MS. FINK: Same objection.
THE WITNESS: I don't know. I'm not sufficiently familiar with the manipulation of the data.
MR. OLIVER: Q. So is it fair to say, then, that you wouldn't know if a netlist is essential to the production of an ultimate ASIC or IC?
MS. FINK: Objection. Mischaracterizes his prior testimony.
THE WITNESS: Yeah. I -- I don't know. I don't think so.
MR. OLIVER: Q. When with you say "I don't think so", what do you mean?
A. Because I think there would be other ways of getting there, of doing the job.
Q. Doing what job?
A. Than having a netlist.
Q. What are those other ways?
MS. FINK: Objection. Asked and answered.
THE WITNESS: I don't know, because I don't

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have sufficient familiarity with the design technology.
MR. OLIVER: Q. So you wouldn't know one way or another if a netlist is essential to the making of an ASIC.
MS. FINK: Objection. Asked and answered.
THE WITNESS: No.
MR. OLIVER: Can we go off the record for a sec.
(There was an off-the-record discussion.)
(A break was taken.)
MR. OLIVER: Q. Just a few more questions.
Your declaration does cover both the design and the production phases and so I just wanted to get an overview from you of -- to summarize that entire process, at least to the best of your understanding.
Starting with the input of the -- an input description of the ASIC to be designed. What happens?
MS. FINK: Objection. Lack of foundation. His declaration does not cover the design phase.
THE WITNESS: I merely refer to ASIC design and manufacturing as separate phases.
MR. OLIVER: Q. But you have an understanding of the design phase from your experience?
A. Only very superficially.
Q. Okay. To the best of your understanding, the

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input of a description of an ASIC to be designed is fed into a design software tool; is that your understanding?
MS. FINK: Objection. Exceeds the scope of this deposition and his declaration.
THE WITNESS: Yes. As far as I know.
MR. OLIVER: Q. And that produces a netlist. Is that your understanding?
MS. FINK: Objection. Same objection. Calls for speculation.
THE WITNESS: I'm not sure. I've lost track what has throughout the whole design cycle.
MR. OLIVER: Q. And the netlist is fed into a tool that creates the mask data, is that correct?
MS. FINK: Same objections.
THE WITNESS: Yes. That is stated in the patent, and that's all I know.
MR. OLIVER: Q. And the mask data is used to produce a mask, is that correct?
A. Yes, mask data is used to produce a mask.
Q. The mask data is fed into what we -- what we discussed, something that receives the tape-out, and the tape-out is used to create a mask, is that correct?
A. Yes.
Q. And at that point you would be very familiar with what happens in the remainder of the flow, is that

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correct?
A. Yes.
Q. So could you summarize what happens at that point? What happens to the mask?
MS. FINK: Objection. Vague and ambiguous as to "what happens to".
THE WITNESS: The tape-out is used by a mask vendor to produce the masking plates, which is a very long process, a very elaborate process. Then those plates would be -- they'd be carefully examined, measurements made, defects looked for, and those plates would then be sent to the wafer fabrication facility and used to make the silicon chips.
MR. OLIVER: Q. Then what happens to the chips?
MS. FINK: Objection. Vague and ambiguous.
THE WITNESS: Yeah. At the end of the wafer fabrication cycle, the chips are tested on the wafer. There are many chips on most wafers, hundreds, thousands in some cases, and chips can be electrically evaluated while sitting on the wafer. There are special tools with very fine probes for making contact with the chips, and many measurements can be made at that stage to test the chip you have just made.
MR. OLIVER: Q. And if you find out there's

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something wrong with the chip you just made, do you have to re-do the netlist?
A. I can't answer that question. I don't know if that would be necessary. It would depend on the nature of the defect, is my guess.
Q. Assuming there's no defect found in the wafer fabrication process, would you have to re-do the netlist?
MS. FINK: Objection. Calls for speculation. He didn't opine as to design.
THE WITNESS: I don't know.
MR. OLIVER: Q. Would you have to re-do the mask data?
MS. FINK: Objection. Calls for speculation.
THE WITNESS: Probably. It may be needed; it may not.
MR. OLIVER: Q. When would it not be needed?
A. If the -- if there was a problem with the data which resulted in the mask maker making plates with the incorrect geometries.
Q. So if there was a malfunction with the chip that was made and there was no problems with either the mask or the wafer fabrication process, would you have to re-do the mask data?
MS. FINK: Same objection. Incomplete

hypothetical. Calls for speculation.
THE WITNESS: I don't know.
MR. OLIVER: Q. Is there any other possibility?
A. Repeat the beginning of that -- the question there again.
Q. If there was a malfunction with the IC or ASIC that was made, assuming there is no problem with the wafer fabrication or any problem with the mask itself --
A. Yes.
Q. -- would you have to re-do the mask data?
MS. FINK: Same objections.
THE WITNESS: I don't know. I'm trying to think of other things which could create a problem. I can't think of other possibilities, but I think there are other possibilities where the mask data would not need to be redone.
MR. OLIVER: Q. Such as what?
A. You had -- you said -- assume there was no problem with the masks, then -- they're perfect, as the mask data indicated they should be, and the wafer fabrication was normal, then mask data would need to be redone probably.
Q. And I think we discussed before that, to get mask data, you would have to produce a netlist either

through some design software or manually, is that correct.
MS. FINK: Objection. Misstates his prior testimony. He didn't say that.
MR. OLIVER: Q. Let me ask you directly. If you needed to re-do a mask, you would be required to do a netlist, whether the netlist was generated manually or through some design software, is that correct?
MS. FINK: Objection. Misstates his testimony. He didn't say you had to have a netlist.
THE WITNESS: Probably not. Probably you would not need to redo the netlist.
MR. OLIVER: Q. If you were to re-do a mask data, you're saying you won't need to re-do a netlist?
A. That's possible.
Q. How is that possible?
A. Because of the conversion from the netlist to the mask data.
Q. Can you explain that in detail?
MS. FINK: Objection. Vague and ambiguous.
MR. OLIVER: Are you objecting to the answer or the question?
MS. FINK: I would be objecting to the question.
THE WITNESS: There can be many problems with a

mask that's been made from the mask data, but it doesn't mean that there's something wrong with the netlist. The netlist, as we discussed earlier, is having the right cells with the wiring defined between those cells to get the function that you need, so the -- in that sense, the wiring -- the circuit schematic should be okay. It doesn't mean the mask data will produce the good circuit. So you may not need to re-do the netlist.
MR. OLIVER: Q. I see.
A. The wiring may be okay, but perhaps some of the dimensions that were converted from the netlist cells, perhaps those dimensions are not correct in the final version.
Q. So, assuming that the creation of the mask data from the original netlist was correct, would you then say that -- if you needed to change the mask data, you would have to change the netlist?
MS. FINK: Objection. Incomplete hypothetical.
THE WITNESS: That would depend on what was wrong with the mask data.
MR. OLIVER: Q. Assuming there was nothing wrong with the translation of the netlist into the mask data, knowing that you would have to change the mask data because of a malfunction in the ultimate ASIC that was made, would you agree that the netlist would have to

be changed?
MS. FINK: Same objection. Incomplete hypothetical.
THE WITNESS: Yeah. I don't know that that interaction between the netlist and the mask data -- and understand it well enough to know if you would have to go back to the netlist or not.
MR. OLIVER: Q. But you know that the netlist is fed into a tool that goes into the mask data, is that correct?
A. Yes.
MR. OLIVER: Okay. Subject to the production of the documents which were not previously produced, I believe that I have no more questions at this time, and hopefully we won't have to call you back.
THE WITNESS: Okay.
MR. OLIVER: Thank you very much.
(The deposition concluded at 12:16 p.m.)

I declare under penalty of perjury that the foregoing is true and correct. Subscribed at _____, California, this _____ day of _____, 2005.

_____
Michael Heynes

STATE OF CALIFORNIA)
) ss.
COUNTY OF SAN FRANCISCO)

CERTIFICATE OF REPORTER

I, JUDIE A. NICHOLAS, a Certified Shorthand Reporter, hereby certify that the witness in the foregoing deposition was by me duly sworn to tell the truth, the whole truth and nothing but the truth in the within-entitled cause;

That said deposition was taken down in shorthand by me, a disinterested person, at the time and place therein stated, and that the testimony of the said witness was thereafter reduced to typewriting, by computer, under my direction and supervision.

I further certify that I am not of counsel or attorney for either or any of the parties to the said deposition, nor in any way interested in the event of this cause, and that I am not related to any of the parties thereto.

DATED: _____, 2005

_____
Judie A. Nicholas, CSR 12229

Westlaw.

Not Reported in F.Supp.2d
Not Reported in F.Supp.2d, 2004 WL 406640 (S.D.N.Y.), 71 U.S.P.Q.2d 1118
(Cite as: 2004 WL 406640 (S.D.N.Y.))

H

Motions, Pleadings and Filings

United States District Court,
S.D. New York.
AT & T CORP., Plaintiff,
v.
MICROSOFT CORPORATION, Defendant.
No. 01 Civ.4872(WHP).

March 5, 2004.

Background: Owner of reissue patent for speech encoding technology brought patent infringement action, and alleged infringer asserted claims for declaratory judgment of noninfringement, invalidity, and unenforceability. Alleged infringer moved for partial summary judgment, seeking to exclude sales of goods incorporating foreign-replicated copies of its alleged infringing software from any damages award.

Holdings: The District Court, Pauley, J., held that:
(1) alleged infringer's export of master disks containing its operating system software constituted supplying of "component" under patent statute, and
(2) foreign-replicated copies of alleged infringer's operating system software constituted components supplied from United States under patent statute.
Motion denied.

West Headnotes

[1] Patents 259(3)
291k259(3) Most Cited Cases
That master disks used by software company to ship its allegedly infringing operating system software to foreign manufacturers to install foreign-replicated copies of software onto foreign-assembled computers were not themselves incorporated into end product abroad did not insulate company from liability under statute treating as patent infringement the assembly of any component of patented invention, supplied from United States, into product outside of United States. 35 U.S.C.A. § 271(f).

[2] Patents 259(3)
291k259(3) Most Cited Cases
Manufacture
Software can be a component of a patented invention or infringing device, within meaning of statute extending United States patent laws to products manufactured abroad from domestically made components. 35 U.S.C.A. § 271(f).

[3] Patents 259(3)
291k259(3) Most Cited Cases
Software company's export of master disk containing its allegedly infringing operating system software constituted supplying of "component" under statute treating as patent infringement the assembly of any component of patented invention, supplied from United States, into product outside of United States, notwithstanding company's contention that "component" did not include intangible information and thus did not apply to software. 35 U.S.C.A. § 271(f).

[4] Patents 259(3)
291k259(3) Most Cited Cases
Manufacture
Foreign-replicated copies of company's allegedly infringing operating system software constituted "components" supplied from United States, for purposes of liability under patent statute treating as infringement the supplying of infringing components from United States for incorporation abroad into finished product that would infringe patent if assembled in United States, given that software, or object code, was originally manufactured in United States and copied abroad for efficiency reasons, and was not created abroad. 35 U.S.C.A. § 271(f).

Patents 328(4)
291k328(4) Most Cited Cases
32,580. Cited.
Jonathan G. Graves, Frank V. Pietrantonio, Brian M. Koide, Cooley Godward, LLP, Reston, VA, for Plaintiff.

Stephen C. Neal, Cooley Godward, LLP, Palo Alto, CA, for Plaintiff.

Robert D. Kaplan, Hallie B. Levin, Friedman Kaplan Seiler & Adelman LLP, New York, NY, for Plaintiff.

Laura A. Kaster, Dina Mack, AT & T Corp., Bedminster, NJ, for Plaintiff, of counsel.

Dale M. Heist, David R. Bailey, Paul B. Milcetic,

Woodcock, Washburn, Kurtz, MacKiewicz & Norris LLP, Philadelphia, Pennsylvania, for Defendant.

James H. Carter, Sullivan & Cromwell, New York, NY, for Defendant.

T. Andrew Culbert, Microsoft Corporation, Redmond, WA, for Defendant, of Counsel.

MEMORANDUM AND ORDER

PAULEY, J.

***1** On June 4, 2001, plaintiff AT & T Corp. ("AT & T") filed this patent infringement action alleging that certain of defendant Microsoft Corporation's ("Microsoft") products containing speech codecs [FN1] infringe its United States Reissue Patent No. 32,580 (the "580 patent"). [FN2] Currently before this Court is Microsoft's motion for partial summary judgment [FN3] to exclude sales of goods incorporating foreign-replicated copies of its infringing Windows software [FN4] from any damages award, pursuant to 35 U.S.C. § 271(f). For the reasons set forth below, Microsoft's motion is denied.

FN1. "A speech codec is a software program that is capable of coding--converting a speech signal into a more compact code--and decoding-- converting the more compact code back into a signal that sounds like the original speech signal." Amended Complaint ("Am.Compl.") ¶ 14.

FN2. Familiarity with this Court's prior Memoranda and Orders is presumed. *See, e.g., AT & T Corp. v. Microsoft Corp.*, 01 Civ. 4872(WHP), 2003 WL 21459573 (S.D.N.Y. June 24, 2003) (construing claims in the 580 patent); *AT & T Corp. v. Microsoft Corp.*, 01 Civ. 4872(WHP) (S.D.N.Y. Sept. 3, 2003) (amending construction of the term "representative"); *AT & T Corp. v. Microsoft Corp.*, 290 F.Supp.2d 409 (S.D.N.Y.2003) (granting partial summary judgment limiting damages pursuant to the patent marking statute, 35 U.S.C. § 287(a)); *AT & T Corp. v. Microsoft Corp.*, 01 Civ. 4872(WHP), 2004 WL 188078 (S.D.N.Y. Feb. 2, 2004) (granting partial summary judgment prohibiting Microsoft from asserting the defenses of equitable estoppel and implied license); *AT & T Corp. v. Microsoft Corp.*, 01 Civ. 4872(WHP), 2004 WL 232725 (S.D.N.Y. Feb. 9, 2004) (granting partial summary judgment prohibiting Microsoft from asserting the defense and counterclaim of inequitable conduct); *AT & T Corp. v. Microsoft Corp.*, 01 Civ. 4872(WHP), 2004 WL 292321 (S.D.N.Y. Feb. 17, 2004) (denying partial summary judgment on invalidity); *AT & T Corp. v. Microsoft Corp.*, 01 Civ. 4872(WHP), 2004 WL 309150 (S.D.N.Y. Feb. 19, 2004) (amending construction for term "excitation").

FN3. Microsoft originally styled this motion as one *in limine* to exclude evidence of foreign sales. On March 4, 2004, the parties stipulated in open court to convert the motion to one for partial summary judgment. (Trial Transcript, dated March 4, 2004 ("Trial Tr .") at 1063-64.)

FN4. For purposes of this motion only, this Court assumes that the object code and software at issue infringe AT & T's 580 patent.

This case presents a novel issue regarding the application of Section 271(f) with profound ramifications for Microsoft and other United States software manufacturers. In the end, the issue of liability under Section 271(f) for foreign replication of infringing software supplied from the United States is a question of law ripe for review by the Federal Circuit.

BACKGROUND

The facts underlying this motion are not in dispute, and are drawn from a Stipulated Statement of Facts, dated March 4, 2004, and marked as Court Exhibit 1. (Trial Tr. at 1064.) Microsoft conceives, writes, compiles, tests, debugs and creates a master version of its Windows operating system software in Redmond, Washington. Microsoft makes a limited number of "golden master" disks in the United States on which the machine-readable object code [FN5] for the Windows operating system software is stored. Some golden master disks are shipped abroad to foreign computer manufacturers, known as foreign "original equipment manufacturers," or "OEMs". Pursuant to licensing agreements with Microsoft, those foreign OEMs use the golden master disks to install foreign-replicated copies of the Windows operating system software onto foreign-assembled computers. While each OEM receives a single golden master disk, that disk is never installed on a computer

sold to consumers. Instead, the golden master disk is used by the OEM to obtain and then replicate object code to install on foreign-assembled computers.

> FN5. According to Microsoft Corporation, its software engineers develop a source code, which is the "human readable form of the software." The source code is put through a compiler which transforms it into object code. Object code is merely the "machine readable version" of the source code in the form of ones and zeros. The object code is then burned onto the golden master disk by a laser for easier transport abroad. (Transcript of Oral Argument, dated December 12, 2003 ("Tr.") at 5-6.) *See also Microsoft Corp. v. Comm'r of Internal Revenue*, 311 F.3d 1178, 1181, 1187 (9th Cir.2002) (describing golden masters).

Microsoft also ships golden master disks to Microsoft-authorized foreign "replicators" who make copies of the Windows operating system software object code and ship those foreign-replicated copies to foreign computer manufacturers.

Additionally, Microsoft supplies its Windows operating system object code from the United States to certain foreign OEMs and authorized foreign replicators by sending them a single encrypted electronic transmission of the object code that was created in the United States. The foreign OEMs and replicators decrypt the transmission and install copies of the object code for the Windows operating system software onto computer hardware to form computer systems, and optionally create CDs or other media containing a foreign-replicated copy of the object code.

During the time relevant to this action, the golden master disks and the encrypted electronic transmissions that Microsoft sends overseas included copies of the accused codecs that infringe AT & T's 580 patent. Microsoft acknowledges that it ships the golden masters and sends the encrypted electronic transmissions containing the infringing object code with the intent and knowledge that the software will be installed on foreign-manufactured computers. Microsoft further acknowledges that it ships the golden masters and encrypted electronic transmissions containing the infringing object code with the intent that the foreign OEMs and authorized replicators will make copies of the object code for the Windows operating system and install those copies onto computer hardware. This computer hardware is manufactured overseas and the completed systems containing the object code created in the United States are then sold to end-users overseas. The parties agree that, other than the object code contained on the golden master disks and the encrypted electronic transmissions of Windows object code, Microsoft does not supply any other "component" from the United States for assembly abroad. Additionally, Microsoft acknowledges that the copying of the software from the golden master disks and the encrypted electronic transmissions overseas is an essential part of the manufacturing process abroad for computers containing Windows. (Tr. at 9.)

***2** AT & T alleges that Microsoft's foreign sales of its Windows software containing the allegedly infringing codecs constitute acts of infringement under 35 U.S.C. § 271(f) that trigger liability and damages. Microsoft contends that Section 271(f) does not attach liability to foreign-replicated copies of its object code because it falls outside the purview of Section 271(f)'s prohibition on foreign assembly of infringing goods. Specifically, Microsoft argues that the object code or software contained on the golden master disks is merely "intangible information," and thus not a "component" as contemplated by Section 271(f). Additionally, Microsoft argues in its reply brief that Section 271(f) does not attach liability to foreign-replicated copies of the software or object code because the copies themselves are not "supplied from" the United States. Microsoft's arguments are without merit.

I. *Summary Judgment Standard*

Rule 56(c) of the Federal Rules of Civil Procedure provides that summary judgment "shall be rendered forthwith if the pleadings, depositions, answers to interrogatories and admissions on file, together with the affidavits, if any, show there is no genuine issue as to any material fact and that the moving party is entitled to judgment as a matter of law." Fed.R.Civ.P. 56(c); *accord Celotex Corp. v. Catrett*, 477 U.S. 317, 322, 106 S.Ct. 2548, 91 L.Ed.2d 265 (1986); *Anderson v.. Liberty Lobby, Inc.*, 477 U.S. 242, 247, 106 S.Ct. 2505, 91 L.Ed.2d 202 (1986). The burden of demonstrating the absence of any genuine dispute as to a material fact rests with the moving party. *See, e.g., Adickes v. S.H. Kress & Co.*, 398 U.S. 144, 157, 90 S.Ct. 1598, 26 L.Ed.2d 142 (1970); *Grady v. Affiliated Cent., Inc.*, 130 F.3d 553, 559 (2d Cir.1997). The movant may meet this burden by demonstrating a lack of evidence to support the nonmovant's case on a material issue on which the nonmovant has the burden of proof. *Celotex*, 477

U.S. at 323.

To defeat a summary judgment motion, the nonmoving party must do "more than simply show that there is some metaphysical doubt as to the material facts." *Matsushita Elec. Indus. Co. v. Zenith Radio Corp.*, 475 U.S. 574, 586, 106 S.Ct. 1348, 89 L.Ed.2d 538 (1986). Indeed, the nonmoving party must "set forth specific facts showing that there is a genuine issue for trial." Fed.R.Civ.P. 56(e); *accord Matsushita Elec.*, 475 U.S. at 587. In evaluating the record to determine whether there is a genuine issue as to any material fact, the "evidence of the nonmovant is to be believed and all justifiable inferences are to be drawn in his favor." *Liberty Lobby*, 477 U.S. at 255; *accord Schering Corp. v. Geneva Pharms.*, 339 F.3d 1373, 1377 (Fed.Cir.2003).

II. *Section 271(f) of the Patent Act*

Section 271(f) of the Patent Act was enacted to prevent infringers from escaping liability under United States patent law by manufacturing or supplying a component of a patented invention from the United States and exporting it for combination into an end product overseas. *Imagexpo, L.L.C. v. Microsoft Corp.*, No. Civ. A. 3:02CV751, 2003 WL 23147556, at *1 (E.D.Va. Aug.19, 2003); *accord* 35 U.S.C. § 271(f); *Aerogroup Int'l, Inc. v. Marlboro Footworks, Ltd.*, 955 F.Supp. 220, 232 (S.D.N.Y.1997) (citing *Windsurfing Int'l, Inc. v. Fred Ostermann GmbH*, 668 F.Supp. 812, 820-21 (S.D.N.Y.1987), *aff'd*, 1 F.3d 1214 (Fed.Cir.1993)); H.R. 6286, Patent Law Amendments Act of 1984, Congressional Record, Oct. 1, 1984, 28069 at H10525-6 ("Legislative History") (Section 271(f) "prevent[s] copiers from avoiding U.S. patents by supplying components of a patented product in this country so that the assembly of the components may be completed abroad."). Components supplied from foreign countries and incorporated into foreign-assembled products do not implicate Section 271(f). *Aerogroup Int'l*, 955 F.Supp. at 232. Section 271(f) states:

> ***3** (1) Whoever without authority supplies or causes to be supplied in or from the United States all or a substantial portion of the components of a patented invention, where such components are uncombined in whole or in part, in such manner as to actively induce the combination of such components outside of the United States in a manner that would infringe the patent if such combination occurred within the United States, shall be liable as an infringer.
>
> (2) Whoever without authority supplies or causes to be supplied in or from the United States any component of a patented invention that is especially made or especially adapted for use in the invention and not a staple article or commodity of commerce suitable for substantial noninfringing use, where such component is uncombined in whole or in part, knowing that such component is so made or adapted and intending that such component will be combined outside of the United States in a manner that would infringe the patent if such combination occurred within the United States, shall be liable as an infringer.

35 U.S.C. § 271(f).

Under paragraph (1) components may be staple articles or commodities of commerce which are also suitable for substantial non-infringing use, but under paragraph (2) the components must be especially made or adapted for use in the invention. *See Bristol-Myers Squibb v. Rhone-Poulenc Rorer, Inc.*, 95 Civ. 8833 (RPP), 2001 WL 1263299, at *4-5 (S.D.N.Y. Oct. 19, 2001). Additionally, paragraph (2) requires the infringer to have an intent that a component "will be combined outside of the United States in a manner that would infringe if the combination occurred within the United States." 35 U.S.C. § 271(f)(2). "Actual combination or assembly of the components by the alleged infringer [is] not required" to trigger liability under Section 271(f). *Waymark Corp. v. Porta Sys. Corp.*, 334 F.3d 1358, 1361 (Fed.Cir.2003). Here, it is undisputed that Microsoft's object code is especially made and supplied from the United States for use in its Windows operating system, that Microsoft intended the components to be combined outside of the United States, and that Microsoft intended that the infringing object code be directly incorporated as an essential part of the foreign-manufactured computers. (Court Ex. 1; Tr. at 9.)

Congress enacted Section 271(f) in response to *Deepsouth Packing Co. v. Laitram Corp.*, 406 U.S. 518, 92 S.Ct. 1700, 32 L.Ed.2d 273 (1972), where the Supreme Court recognized a "loophole" in infringement law allowing copiers to escape liability by finalizing assembly of products outside the United States. *See* H.R. 6286, Patent Law Amendments Act of 1984, Congressional Record, Oct. 1, 1984, 28069, H10525-6. In *Deepsouth*, the Supreme Court held that manufacturing components of a patented invention in the United States, but assembling those components into the patented invention outside the United States, was not "making," and thus did not constitute infringement under Section 271(a) of the

Patent Act. 406 U.S. at 527-28. In the wake of *Deepsouth,* Congress enacted Section 271(f) to prevent infringers from exploiting that loophole. *See* H.R. 6286, Patent Law Amendments Act of 1984, Congressional Record, Oct. 1, 1984, 28069, H10525-6. The legislative history of Section 271(f) reads in pertinent part:

> ***4** Part of the subcommittee's job is to secure for the owners of intellectual property, including patent holders, a workable, efficient, and vigorous set of laws to protect their creations.... [W]ithout enactment of these housekeeping-oriented measures, *the patent system would not be responsive to the challenges of a changing world* and the public would not benefit from the release of creative genius.... Section 101 [of the Bill] makes two major changes in the patent law in order to avoid encouraging manufacturing outside the United States.... [Section 271(f)] will prevent *copiers* from avoiding U.S. patents by supplying components of a patented product in this country so that the assembly of the components may be completed abroad. This proposal responds to [*Deepsouth*] concerning the need for a legislative solution to close a loophole in patent law.

H.R. 6286, Patent Law Amendments Act of 1984, Congressional Record, Oct. 1, 1984, 28069, H10525 (emphasis added).

Section 271(f) bridges the *Deepsouth* synapse by including as infringement under the Patent Act the assembly of any component of a patented invention, supplied from the United States, into a product assembled outside of the United States. 35 U.S.C. § 271(f). Microsoft does not dispute the construction of Section 271(f), but argues that: (1) its object code or software is not a "component" under Section 271(f); and (2) its foreign-replicated copies are not "supplied from" the United States. Otherwise, Microsoft acknowledges that its actions satisfy the requirements of Section 271(f). (Court Ex. 1.)

III. *Software as a Component*

[1] Microsoft argues that foreign-replicated copies of its Windows operating system software cannot be statutory "components" supplied from the United States to form foreign-assembled computer systems because "the infringing Windows operating system software stored on the golden master disks [and sent electronically] is intangible information," and the golden master disk is "simply a medium for transmission of the software information," and is never incorporated into an end product abroad. (MS Br. at 1; Court Ex. 1.) The object code or software that is contained on each golden master disk or transmitted electronically, as opposed to the golden master disk or method of encrypted transmission itself, is at the heart of the parties' dispute and this Court's analysis. It is undisputed that the infringing software is intentionally shipped abroad for incorporation into foreign-assembled computers. (Court Ex. 1.) Indeed, the golden master disk simply recognizes the economic efficiencies in shipping Microsoft's software abroad, and does not alone insulate Microsoft from liability under Section 271(f). *See Eolas Techs. Inc. v. Microsoft Corp.*, 99 C 0626, 2004 WL 170334, at *3-5 (N.D.Ill. Jan.15, 2004).

[2][3] Microsoft argues that its infringing software must be a "physical product" to constitute a "component" under Section 271(f). As noted, Section 271(f) precludes exportation of certain "component(s)" of patented inventions. 35 U.S.C. § 271(f). Microsoft contends that infringing software transported by golden master disk or through electronic transmission is merely "intangible information," and thus not a "component" as contemplated by Section 271(f). It is well-established, however, that software can be a component of a patented invention or infringing device. *See, e.g., In re Alappat,* 33 F.3d 1526, 1545 (Fed.Cir.1994) ("[A] computer operating pursuant to software may represent patentable subject matter, provided, of course, that the claimed subject matter meets all the other requirements of Title 35."); *Imagexpo, L.L.C. v. Microsoft Corp.*, No. Civ.A 3:02CV751, 2003 WL 23147556 (E.D.Va. Aug.19, 2003) (in examining Microsoft NetMeeting units exported overseas on golden master disks, holding that Microsoft's "code is a patentable apparatus" and that the golden master and code constitute "components" under Section 271(f)); *Eolas Techs. Inc. v. Microsoft Corp.*, 274 F.Supp.2d 972, 973 (N.D.Ill.2003) (holding that the software in a computer product "is, in law, the legal equivalent of a piece of computer hardware and not the legal equivalent of a chemical formula"); *NTP, Inc. v. Research In Motion, Ltd.*, 261 F.Supp.2d 423, 431 (E.D.Va.2002) (noting that defendant supplied "application programs" that are "components combined with [an] Intel processor outside the United States" and especially adapted for use in the infringing product); United States Patent & Trademark Office Manual of Patent Examining Procedure (the "MPEP") § 2106, at 2100-13 (8th ed.2003) (noting that a computer program has functional and structural elements, can be recited as part of a claim, statutory manufacture or machine,

and noting that "[w]hen a computer program is recited in conjunction with a physical structure, such as a computer memory, Office personnel should treat the claim as a *product* claim.") (emphasis added); *see also* Southwest Software, Inc. v. Harlequin Inc., 226 F.3d 1280, 1287-88, 1298-99 (Fed.Cir.2000). Indeed, Microsoft acknowledges that software is patentable (Tr. at 10; MS Reply at 1), and it argued successfully to the Ninth Circuit that its golden master disks that contain the object code at issue here were tangible export property for tax purposes. *Microsoft Corp. v. Comm'r of Internal Revenue*, 311 F.3d 1178, 1185 (9th Cir.2002) (holding that the software or object code contained on the golden master disks was "export property," that only contemplates tangible property, and finding "computer software reproductions similar to 'films, tapes, [and] records" ') (alteration in original). Tellingly, Microsoft retreated from this argument in its reply brief and at oral argument.

***5** Microsoft urges this Court to narrowly interpret the term "component" in Section 271(f) to exclude software or object code. However, there is no limitation of the term "components," either in the statutory text or in the legislative history, to machines or other structural combinations. *W.R. Grace & Co. v. Intercat, Inc.*, 60 F.Supp.2d 316, 320-21 (D.Del.1999) (finding 271(f) liability for supply of chemical composition from the United States for combination with other materials abroad); *see also Moore U .S.A. Inc. v. Standard Register Co.*, 144 F.Supp.2d 188, 195 (W.D.N.Y.2001) (finding paper, glue and blueprints for making envelopes "components" under 271(f)); *Lubrizol Corp. v. Exxon Corp.*, 696 F.Supp. 302, 325 (N.D.Ohio 1988) (same for supply of lubricant additive for combination in a lubricant composition outside the United States). Further, there is nothing in the legislative history of Section 271(f) or in any jurisprudence interpreting it to say that software cannot be a component under Section 271(f). *W.R. Grace*, 60 F.Supp.2d at 321 ("A contrary holding ... would be tantamount to legislating additional language to a statute."). Indeed, excluding protection for inventions using software "would not be responsive to the challenges of a changing world," as software and computers have become an essential part of society and business since the enactment of Section 271(f). H.R. 6286, Patent Law Amendments Act of 1984, Congressional Record, Oct. 1, 1984, 28069, H10525.

Microsoft cites to several cases in support of its contention that software cannot be a component under Section 271(f). (MS Br. at 9-10.) Those cases are distinguishable, as they all involve design or method patents, which have no components, or instructions for assembly of products abroad, which is not a component. *See, e.g.*, *Standard Havens Prods., Inc. v. Gencor Indus., Inc.*, 953 F.2d 1360, 1374 (Fed.Cir.1991) (holding 271(f) inapplicable to a method patent for producing asphalt, "not the apparatus for implementing that process"); *Enpat, Inc. v. Microsoft Corp.*, 6 F.Supp.2d 537, 538-39 (E.D.Va.1998) (finding no 271(f) liability for a method patent with no components where the patent only described steps required to accomplish a task); *Pellegrini v. Analog Devices, Inc.*, C.A. No. 02-11562-RWZ, 2003 WL 21026797, at *1 (D.Mass. May 7, 2003) (finding no 271(f) liability for exportation of instruction for foreign disposal of computer chips); *Aerogroup Int'l*, 955 F.Supp. at 231-32 (Section 271(f) inapplicable for a design patent for a shoe sole where the patent claimed no "components" and the soles were manufactured abroad).

Notably, the two other courts that have considered the precise issue before this Court have held that Microsoft's export of its golden master disks containing infringing code constitutes the supply of a "component" under Section 271(f). *Eolas Techs. Inc. v. Microsoft Corp.*, 274 F.Supp.2d 972 (N.D.Ill.2003), *reconsideration denied*, 2004 WL 170334, at *3-5 (N.D.Ill. Jan.15, 2004); *Imagexpo LLC v. Microsoft Corp.*, 2003 WL 23147556 (E.D.Va. Aug.19, 2003). Additionally, in *NTP, Inc. v. Research in Motion, Ltd.*, 261 F.Supp.2d 423, 436-37 (E.D.Va.2002), a district court granted summary judgment of infringement pursuant to Section 271(f), finding that the defendant's transmission network for its Blackberry wireless email/paging devices manufactured in Canada fell within Section 271(f) because it incorporated domestically-supplied components, such as Microsoft's Exchange Server software, that the defendant combined outside the United States. Microsoft only distinguishes these cases by noting that they were decided before *Bayer AG v. Housey Pharms., Inc.*, 340 F.3d 1367 (Fed.Cir.2003). (Tr. at 18; MS Reply Br. at 6.)

***6** Microsoft argues that *Bayer* compels a finding that it is not liable for infringement and damages for foreign sales of computers containing the infringing software. In *Bayer*, the Federal Circuit addressed the term "component" in Section 271(g) of the Patent Act. *Bayer*, 340 F.3d at 1376- 77. Section 271(g) prohibits importation into the United States of products produced by "patented manufacturing processes, i.e., methods of actually making or

creating a product as opposed to methods of gathering information about, or identifying a substance worthy of further development." *Bayer,* 340 F.3d at 1370. In dicta, the Federal Circuit stated that the term "component" in Section 271(g) "appears to contemplate a physical product." *Bayer,* 340 F.3d at 1376-77. However, Microsoft wrenches the Federal Circuit's comment out of its context; it is not the clear statement of law on Section 271(f) liability that Microsoft would have this Court adopt.

In *Bayer,* the Federal Circuit held that Section 271(g) does not proscribe the transmission of "information" into the United States. 340 F.3d at 1371. The "information" in *Bayer,* however, was markedly different than the software or object code at issue here. The information in *Bayer* was data generated from a patented method to identify whether a given substance had a particular property, namely, whether that substance activated or inhibited protein activity in a cell. *Bayer,* 340 F.3d at 1369. This data could be used to identify effective drugs for treating diseases. The patentee alleged that Bayer used the patented process outside the United States, subsequently imported into the United States *the data generated from that process,* identified effective drugs from that data, and manufactured those drugs in the United States. *Bayer,* 340 F.3d at 1369-70. The Federal Circuit held that importation of the data generated from the patented process did not infringe under Section 271(g) because that Section is directed towards articles of manufacture, and not data or "information" used to identify those articles. *Bayer,* 340 F.3d at 1370. Indeed, the data produced from the patented process abroad was not directly used to manufacture the drugs at issue in the United States. *Bayer,* 340 F.3d at 1369-70.

Bayer' s holding does not advance this Section 271(f) analysis because: (1) *Bayer* only applies to Section 271(g); [FN6] and (2) the "information" or "data processing" that resulted from a patented process in *Bayer* is completely unrelated to the software or object code at issue here. For example, here the software or object code itself is an essential part of the end product and component-assembly abroad. In contrast, in *Bayer* the resulting data created by a patented process was transferred to the United States from abroad and was ultimately used to identify drugs which were then manufactured in the United States. *Bayer,* 340 F.3d at 1368-69. Thus, in *Bayer,* the transmitted "data" at issue was not incorporated into the end-product; it was the result of a patented process, not part of it. In this action, the object code at issue actually contains the patented codecs, which are not derived from a similar method patent, and the infringing code is sent overseas to be incorporated directly into the end-product abroad.

> FN6. Indeed, the only mention of Section 271(f) in *Bayer* is a passing reference to Congress's intent to avoid encouragement of manufacturing infringing goods outside the United States. *Bayer,* 340 F.3d at 1371.

*7 Citing the dicta in *Bayer,* Microsoft argues that the object code contained on the golden master is intangible information, and thus cannot trigger liability under Section 271(f). Microsoft's argument, however, relies heavily on the presumption that the object code on the golden master disks and in the encrypted transmissions is the type of intangible information or data from a patented process that did not trigger Section 271(g) liability in *Bayer.* As noted above, this Court rejects that presumption.

IV. *Foreign-Replicated Copy as a Component*

[4] In its reply brief, Microsoft advances the argument that a foreign-replicated copy of the infringing software does not constitute a "component" supplied from the United States, and thus cannot trigger Section 271(f) liability. This Court heard AT & T's response at oral argument, and agrees with its position.

Microsoft contends that since the object code eventually incorporated into the foreign computers is *replicated abroad,* those foreign-replicated copies cannot be considered to be a component "supplied from" the United States. Specifically, Microsoft argues that the foreign-replicated copies cannot "be said to have been 'supplied' from the U.S. even though they never touched U.S. soil." (MS Reply Br. at 1.) Essentially, Microsoft seeks to equate replication of the object code abroad with the manufacturing or "supply" of it from abroad. Microsoft's argument ignores the undisputed fact that the object code is originally manufactured in the United States, and supplied from the United States to foreign replicators or OEMs with the intention of incorporating such software into foreign-assembled computers. (Court Ex. 1.) The fact that Microsoft ships one golden master disk or sends one electronic transmission with the infringing object code to each foreign OEM, rather than shipping one CD for each computer for efficiency purposes, cannot shield Microsoft from the letter and intent of the statute--to prohibit circumvention of infringement of a United States patent by supplying certain infringing

components from the United States, and shipping them abroad for incorporation into a finished product that would infringe if assembled in the United States. [FN7] *See* 35 U.S.C. 271(f); H.R. 6286, Patent Law Amendments Act of 1984, Congressional Record, Oct. 1, 1984, 28069, H10525; *Imagexpo,* 2003 WL 23147556; *Eolas Techs.,* 2004 WL 170334, at *3-5.

> FN7. Indeed, at oral argument, Microsoft acknowledged that if individual disks with the infringing Windows operating system object code were sent abroad for incorporation into each foreign-assembled computer (rather than one golden master disk), Microsoft would be liable for infringement under Section 271(f). (Tr. at 16, 28.) Under this scenario, Microsoft would be liable for direct infringement under Section 271(f). *NTP,* 261 F.Supp.2d at 436-37.

In support of its argument, Microsoft analogizes its software to a "mold" for tires that is exported to a foreign plant to make tires there for combination with foreign-made cars. Microsoft argues that its software, like the foreign-molded tires, cannot be said to be components of the patented combination "supplied" from the United States because Section 271(f) looks to the place from which the "component" in question was made and supplied. Unlike the tires that are manufactured from a mold, however, the software here has already been manufactured in, and supplied from, the United States and is only copied abroad--the software is not a mold for the creation of another separate type of component. Indeed, there is no evidence before this Court that the foreign-incorporated object code or software is being created anew from instructions concerning a process for creating code abroad. *See Enpat,* 6 F.Supp.2d at 538-39 (finding no 271(f) liability for a method patent with no components where the patent only described steps required to accomplish a task); *Pellegrini,* 2003 WL 21026797, at *1 (finding no 271(f) liability for exportation of instruction for foreign disposal of computer chips). Further, Microsoft's tire mold is devoid of any content until rubber is poured into it and a separate and distinct object, a tire, is created. Here, again, the software itself is the component, or the "tire", rather than a mold.

***8** As noted in *Imagexpo,* the golden master or electronic transmission at issue here contains object code that becomes an essential component of the finished computer product. "In other words, the overseas replicator [or OEMs] do[ ] not simply construct the computer product using a plan, design, or recipe supplied by Microsoft. Instead, the functional nucleus of the finished computer product is driven by the code, which is transmitted through the golden master." *Imagexpo,* 2003 WL 23147556. This Court agrees and finds Microsoft's "tire mold" analogy unpersuasive.

V. *Policy Argument*

Finally, Microsoft advances a "doomsday" policy argument to buttress its position, namely that if Section 271(f) liability attaches to foreign distribution of its infringing software, it "would simply pick up [its] manufacturing operation for the golden master, go [one] hundred miles north to Vancouver, set up the operation in Vancouver, [and] burn [its] golden master CDs [there]." (Tr. at 21-22.) Microsoft asserts that this would be the only option to "reduce by two-thirds our exposure in all of these patent cases" relating to Section 271(f) liability for worldwide sales. [FN8] (Tr. at 22.) Additionally, Microsoft complains that, unlike United States-based companies, foreign software companies do not face Section 271(f) liability, and can sell software world-wide without incurring the same liability in the United States. (Tr. at 22.) While this Court appreciates Microsoft's concerns about a paradigm shift for United States software manufacturers, those concerns are better addressed through manufacture of non-infringing goods or Congressional action, rather than a judicial engraftment on Section 271(f) of the Patent Act.

> FN8. Notably, Microsoft's policy argument does not address distribution of the infringing software through electronic transmission.

CONCLUSION

For the reasons set forth above, defendant Microsoft Corporation's motion for partial summary judgment pursuant to 35 U.S .C. § 271(f) is denied.

Not Reported in F.Supp.2d, 2004 WL 406640 (S.D.N.Y.), 71 U.S.P.Q.2d 1118

Motions, Pleadings and Filings (Back to top)

- 1:01cv04872 (Docket) (Jun. 04, 2001)

END OF DOCUMENT

United States Patent [19]

Kobayashi et al.

[11] **Patent Number: 4,922,432**

[45] **Date of Patent: May 1, 1990**

[54] **KNOWLEDGE BASED METHOD AND APPARATUS FOR DESIGNING INTEGRATED CIRCUITS USING FUNCTIONAL SPECIFICATIONS**

[75] Inventors: **Hideaki Kobayashi**, Columbia, S.C.; **Masahiro Shindo**, Osaka, Japan

[73] Assignees: **International Chip Corporation**, Columbia, S.C.; **Ricoh Company, Ltd.**, Tokyo, Japan

[21] Appl. No.: **143,821**

[22] Filed: **Jan. 13, 1988**

[51] **Int. Cl.**[5] **G06F 15/60**

[52] **U.S. Cl.** **364/490**; 364/489; 364/488; 364/521

[58] **Field of Search** 364/488–491, 364/521, 300, 513

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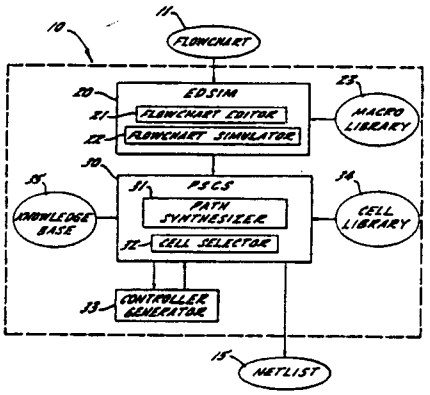
Primary Examiner—Felix D. Gruber
Assistant Examiner—V. N. Trans
Attorney, Agent, or Firm—Bell, Seltzer, Park & Gibson

[57] **ABSTRACT**

The present invention provides a computer-aided design system and method for designing an application specific integrated circuit which enables a user to define functional architecture independent specifications for the integrated circuit and which translates the functional architecture independent specifications into the detailed information needed for directly producing the integrated circuit. The functional architecture independent specifications of the desired integrated circuit can be defined at the functional architecture independent level in a flowchart format. From the flowchart, the system and method uses artificial intelligence and expert systems technology to generate a system controller, to select the necessary integrated circuit hardware cells needed to achieve the functional specifications, and to generate data and control paths for operation of the integrated circuit. This list of hardware cells and their interconnection requirements is set forth in a netlist. From the netlist it is possible using known manual techniques or existing VLSI CAD layout systems to generate the detailed chip level topological information (mask data) required to produce the particular application specific integrated circuit.

20 Claims, 12 Drawing Sheets



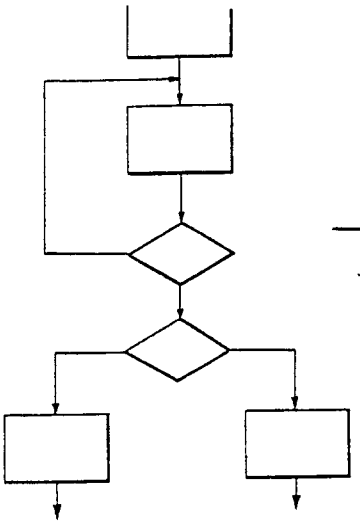


Fig. 1a.
FUNCTIONAL LEVEL

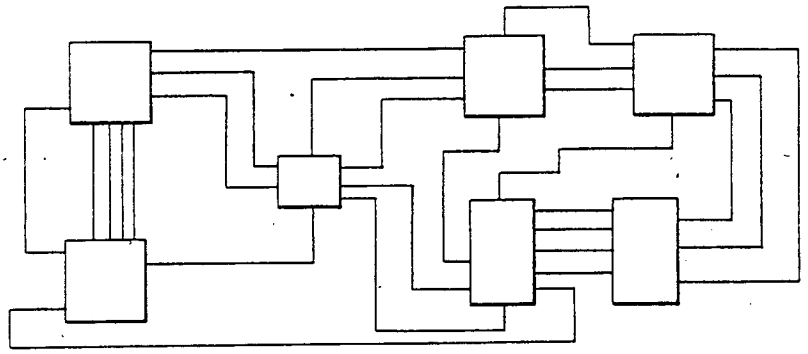


Fig. 1b.
STRUCTURAL LEVEL

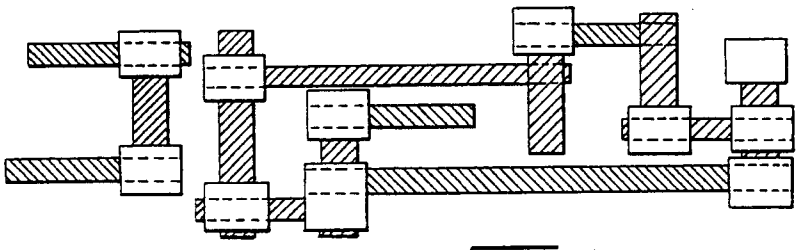


Fig. 1c.
PHYSICAL LAYOUT LEVEL

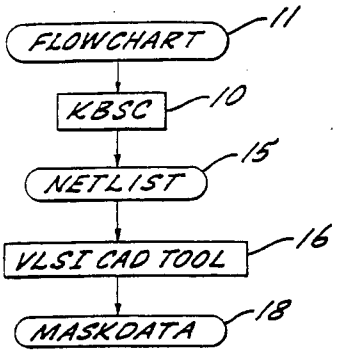

FLOWCHART
11
KBSC
10
NETLIST
15
VLSI CAD TOOL
16
MASKOATA
18

Fig. 2.

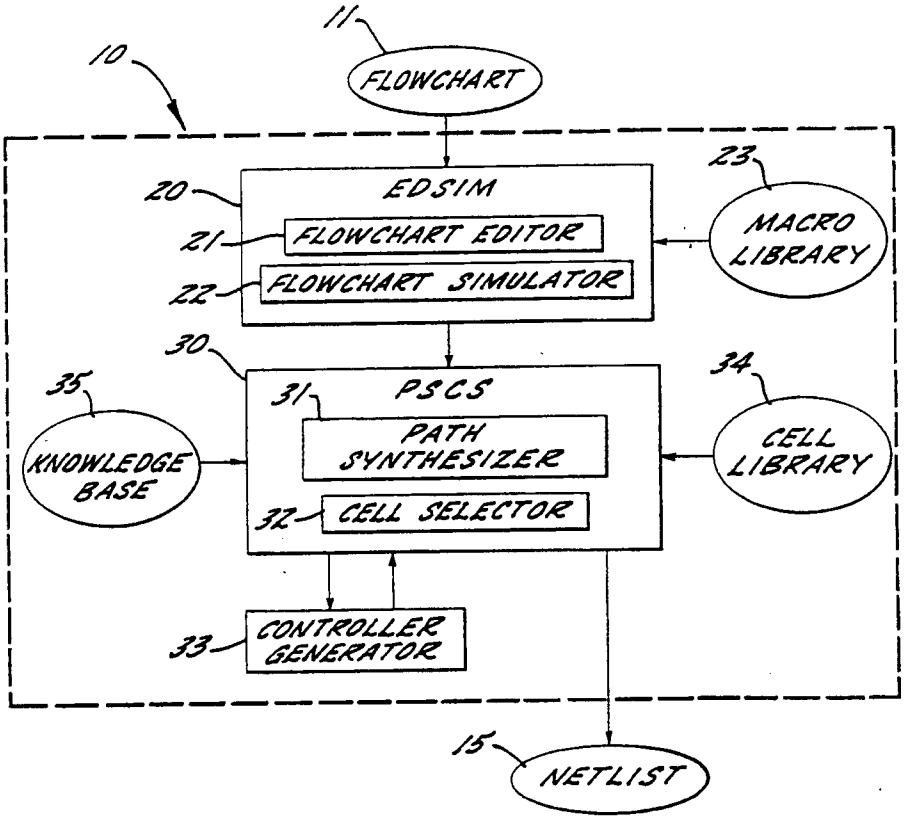

11
FLOWCHART
10
EDSIM
20
FLOWCHART EDITOR
21
FLOWCHART SIMULATOR
22
23
MACRO LIBRARY
30
PSCS
31
PATH SYNTHESIZER
32
CELL SELECTOR
33
CONTROLLER GENERATOR
35
KNOWLEDGE BASE
34
CELL LIBRARY
15
NETLIST

Fig. 3.

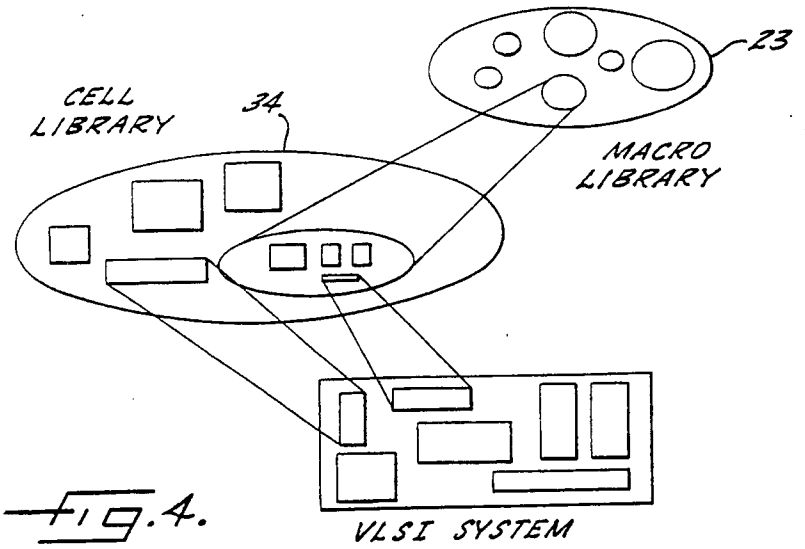

23
CELL LIBRARY
34
MACRO LIBRARY
VLSI SYSTEM

Fig. 4.

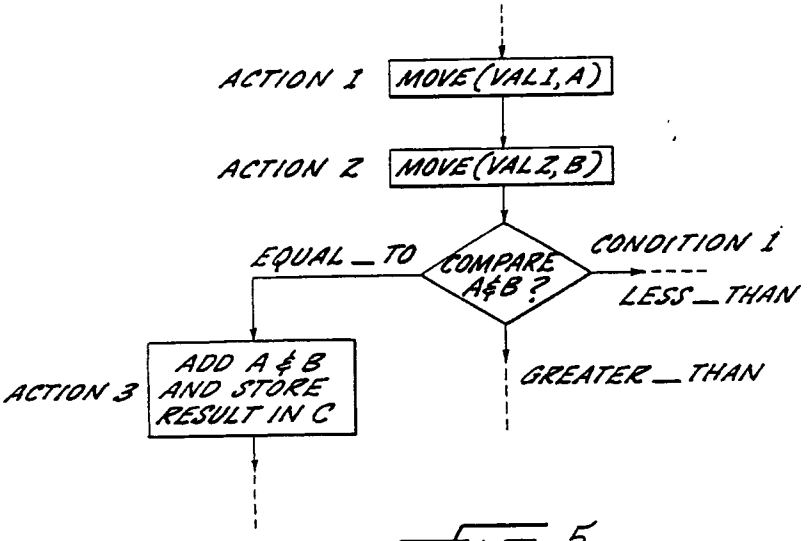

ACTION 1
MOVE(VAL1,A)
ACTION 2
MOVE(VAL2,B)
EQUAL_TO
COMPARE A&B ?
CONDITION 1
LESS_THAN
GREATER_THAN
ACTION 3
ADD A & B AND STORE RESULT IN C

Fig. 5.

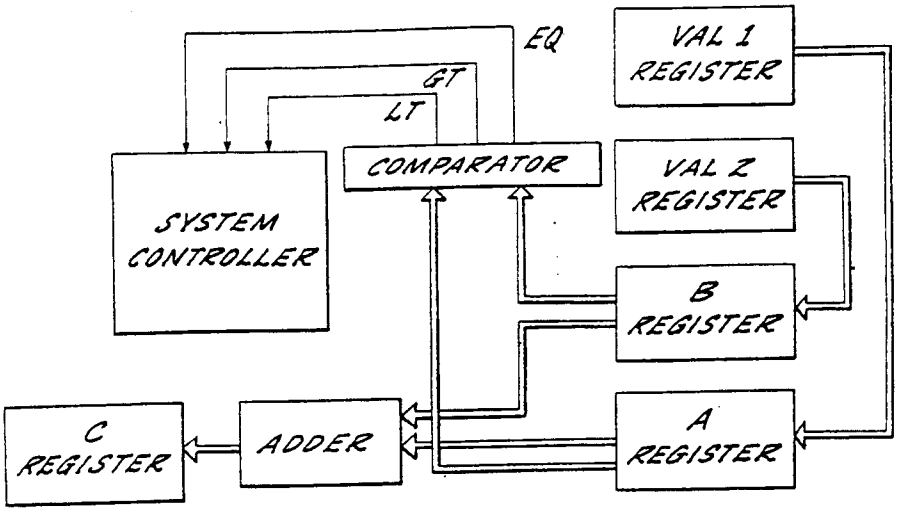

EQ
GT
LT
VAL 1 REGISTER
COMPARATOR
VAL 2 REGISTER
SYSTEM CONTROLLER
B REGISTER
C REGISTER
ADDER
A REGISTER

Fig. 6.

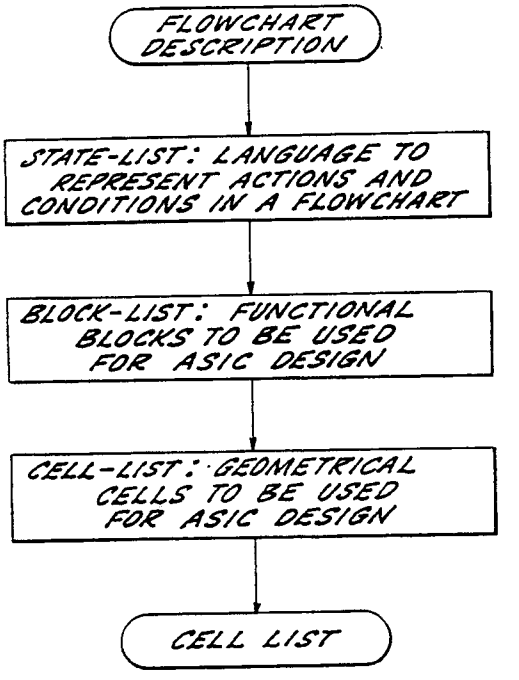

FLOWCHART DESCRIPTION
STATE-LIST: LANGUAGE TO REPRESENT ACTIONS AND CONDITIONS IN A FLOWCHART
BLOCK-LIST: FUNCTIONAL BLOCKS TO BE USED FOR ASIC DESIGN
CELL-LIST: GEOMETRICAL CELLS TO BE USED FOR ASIC DESIGN
CELL LIST

Fig. 9.

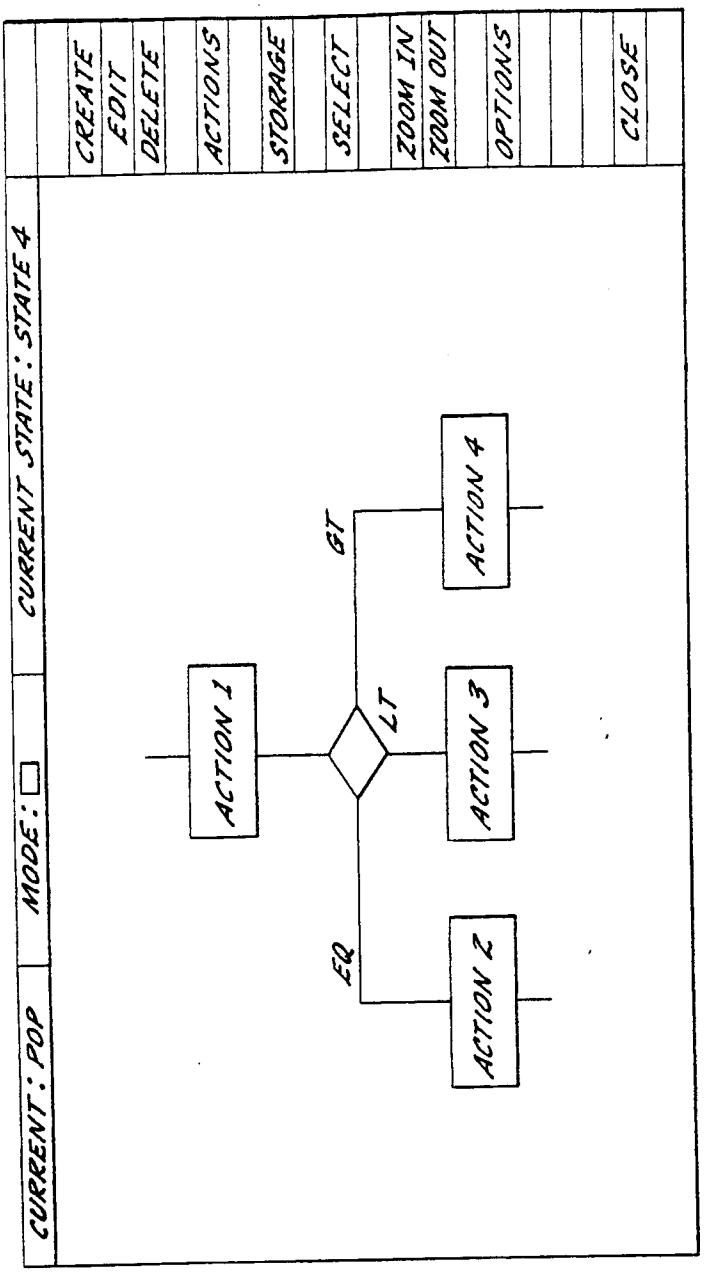

CREATE
EDIT
DELETE
ACTIONS
STORAGE
SELECT
ZOOM IN
ZOOM OUT
OPTIONS
CLOSE
CURRENT STATE: STATE 4
MODE: □
CURRENT: POP
ACTION 1
GT
LT
EQ
ACTION 4
ACTION 3
ACTION 2

FIG. 7.

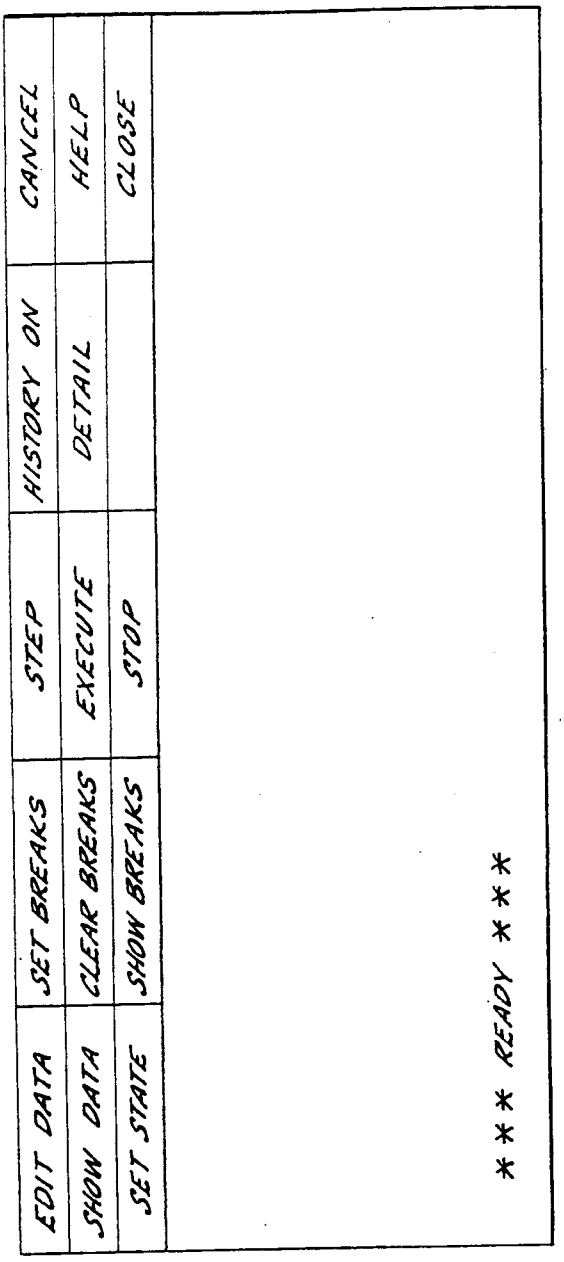

EDIT DATA
SET BREAKS
STEP
HISTORY ON
CANCEL
SHOW DATA
CLEAR BREAKS
EXECUTE
DETAIL
HELP
SET STATE
SHOW BREAKS
STOP
CLOSE
**** READY ****

FIG. 8.

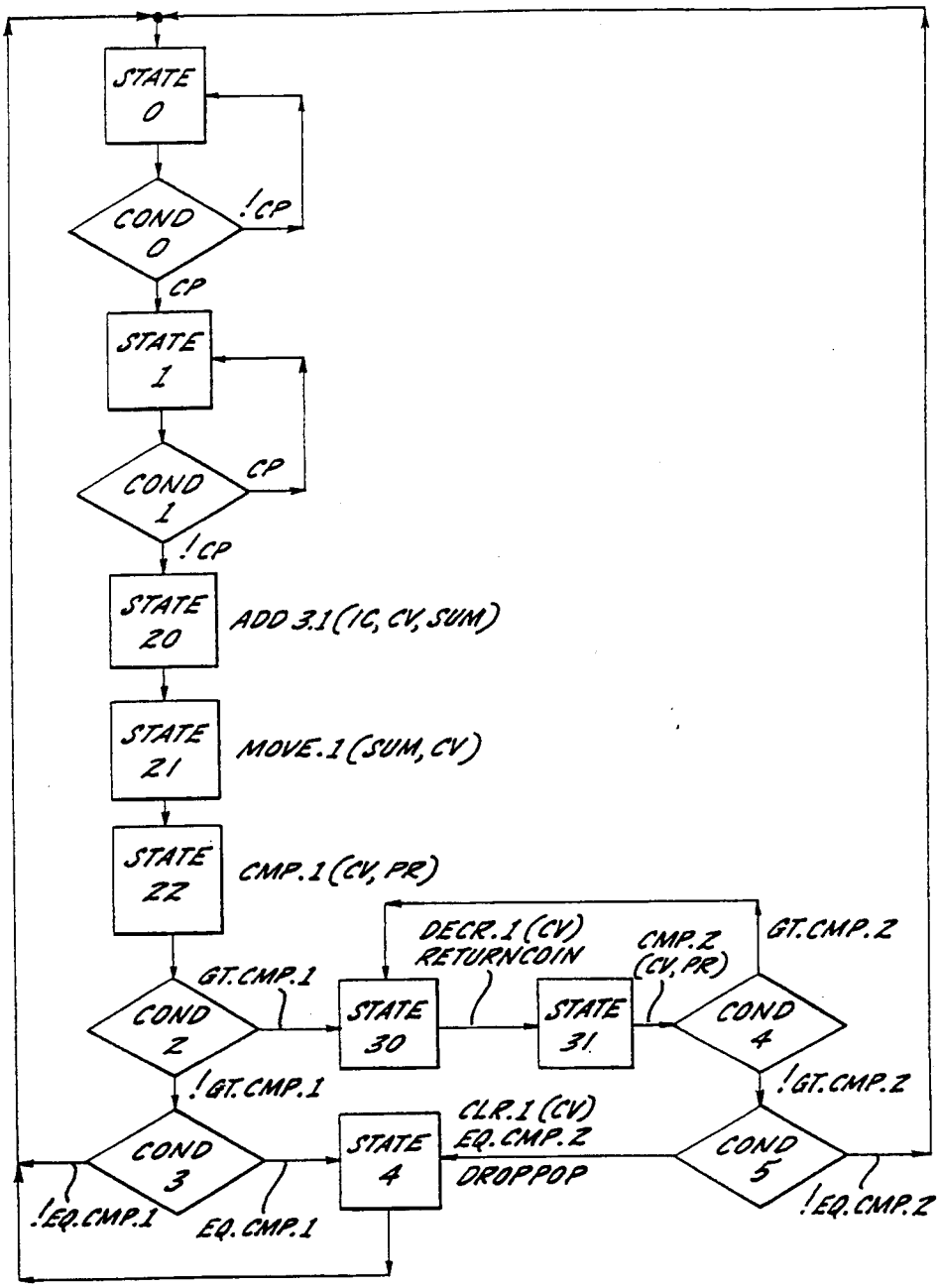

STATE 0
COND 0
!CP
CP
STATE 1
COND 1
CP
!CP
STATE 20
ADD 3.1 (IC, CV, SUM)
STATE 21
MOVE.1 (SUM, CV)
STATE 22
CMP.1 (CV, PR)
GT.CMP.1
COND 2
!GT.CMP.1
STATE 30
DECR.1 (CV)
RETURNCOIN
STATE 31
CMP.2 (CV, PR)
GT.CMP.2
COND 4
!GT.CMP.2
COND 3
!EQ.CMP.1
EQ.CMP.1
STATE 4
CLR.1 (CV)
EQ.CMP.2
DROPPOP
COND 5
!EQ.CMP.2

Fig. 10.

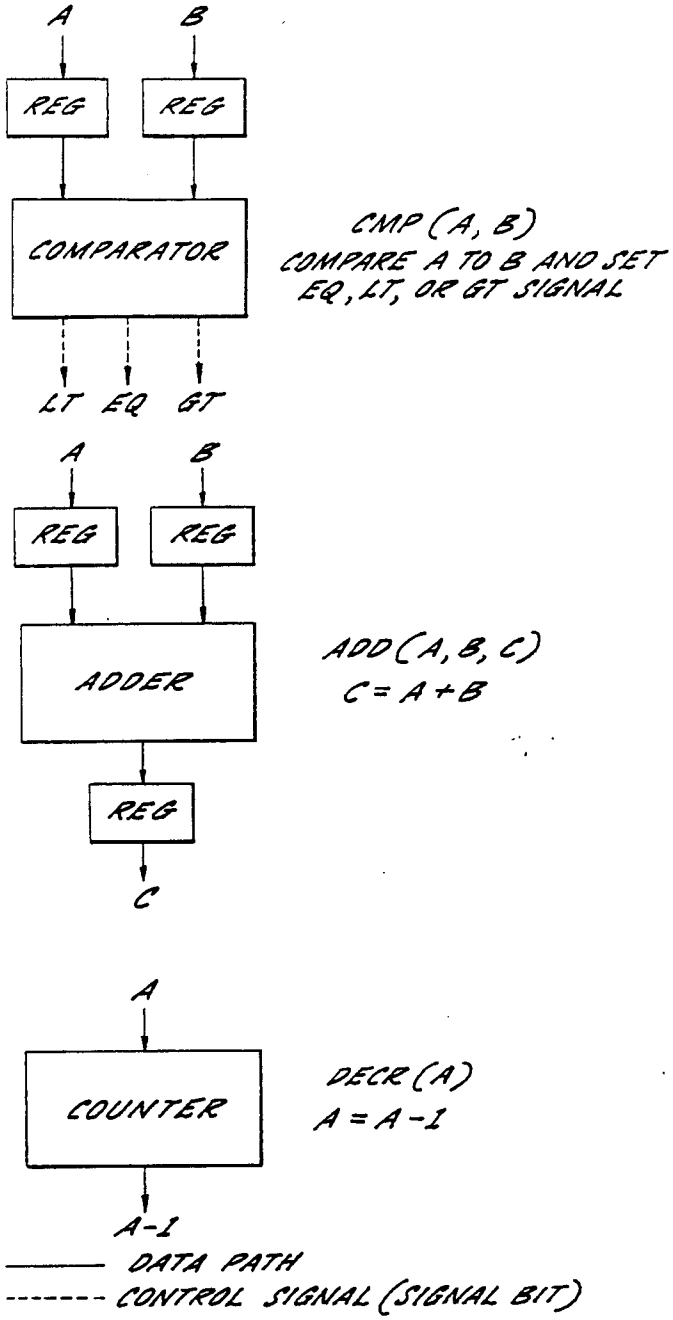

A
B
REG
REG
COMPARATOR
CMP (A, B)
COMPARE A TO B AND SET
EQ, LT, OR GT SIGNAL
LT EQ GT
A
B
REG
REG
ADDER
ADD (A, B, C)
C = A + B
REG
C
A
COUNTER
DECR (A)
A = A - 1
A-1
DATA PATH
CONTROL SIGNAL (SIGNAL BIT)

Fig. 11.

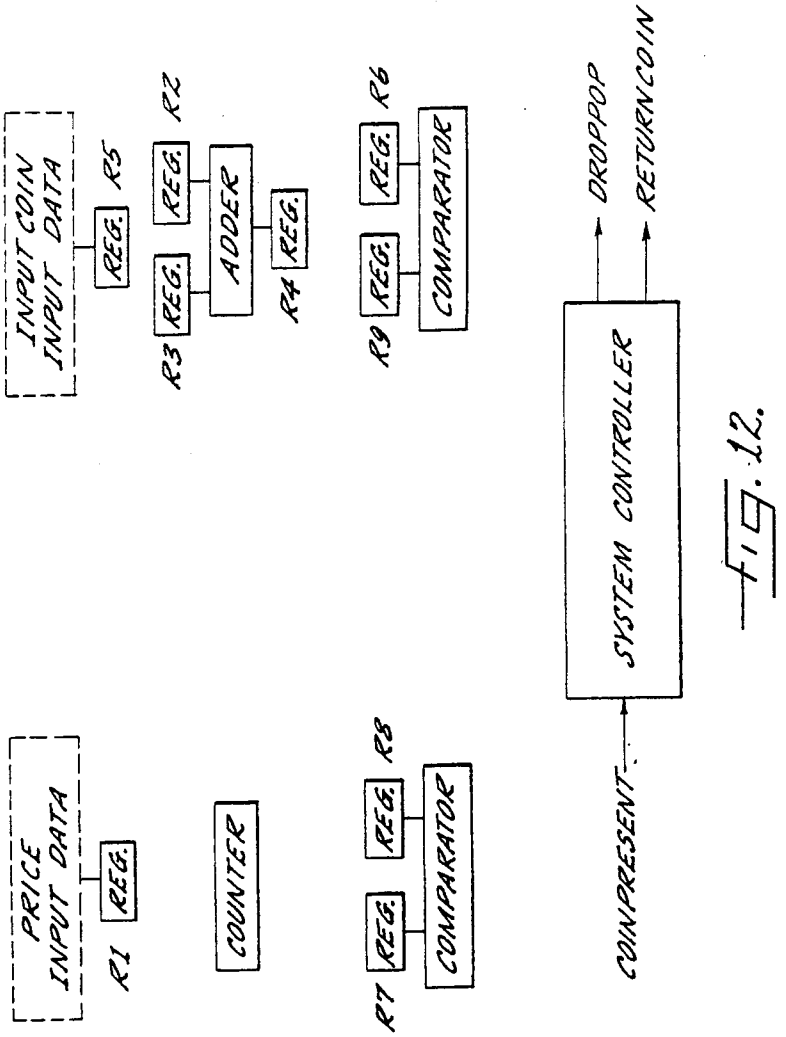

INPUT COIN INPUT DATA
REG.
R5
REG.
R2
REG.
R3
ADDER
R4
REG.
REG.
R6
REG.
R9
COMPARATOR
DROPPOP
RETURN COIN
SYSTEM CONTROLLER
COIN PRESENT
PRICE INPUT DATA
REG.
R1
COUNTER
REG.
R8
REG.
R7
COMPARATOR

FIG. 12.

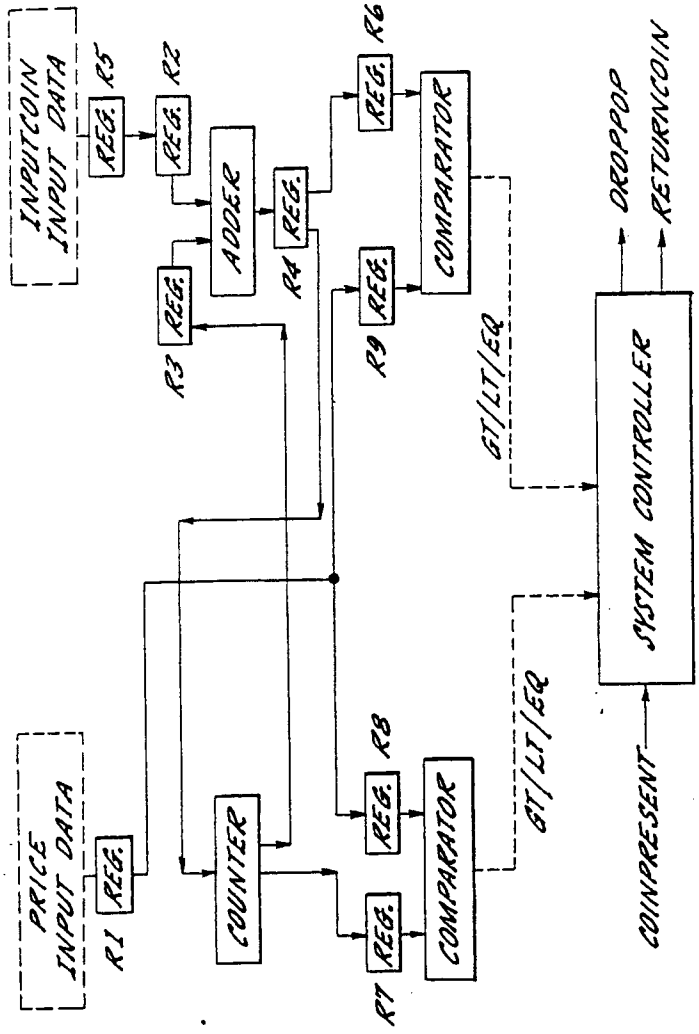

INPUTCOIN INPUT DATA
REG.
R5
REG.
R2
ADDER
REG.
R4
REG.
R6
COMPARATOR
REG.
R3
REG.
R9
GT/LT/EQ
DROPPOP
RETURNCOIN
SYSTEM CONTROLLER
PRICE INPUT DATA
REG.
R1
COUNTER
REG.
R8
REG.
R7
COMPARATOR
GT/LT/EQ
COINPRESENT

FIG. 13.

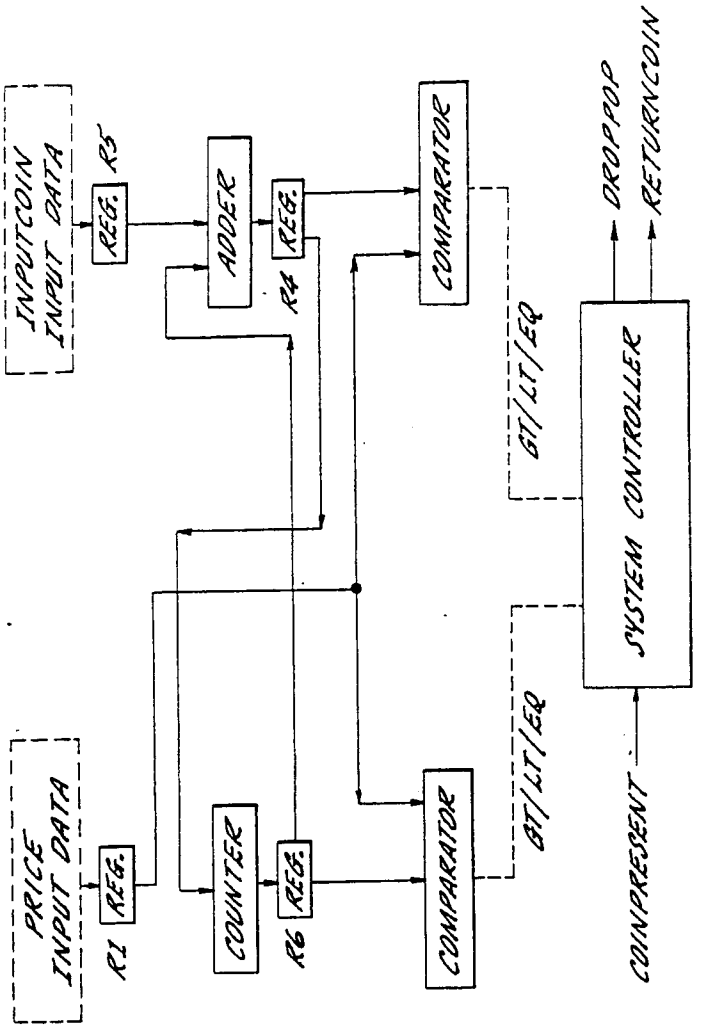

INPUTCOIN
INPUT DATA
REG.
R3
ADDER
REG.
R4
COMPARATOR
GT/LT/EQ
DROPPOP
RETURNCOIN
SYSTEM CONTROLLER
COINPRESENT
PRICE
INPUT DATA
REG.
R1
COUNTER
REG.
R6
COMPARATOR
GT/LT/EQ

FIG. 14.

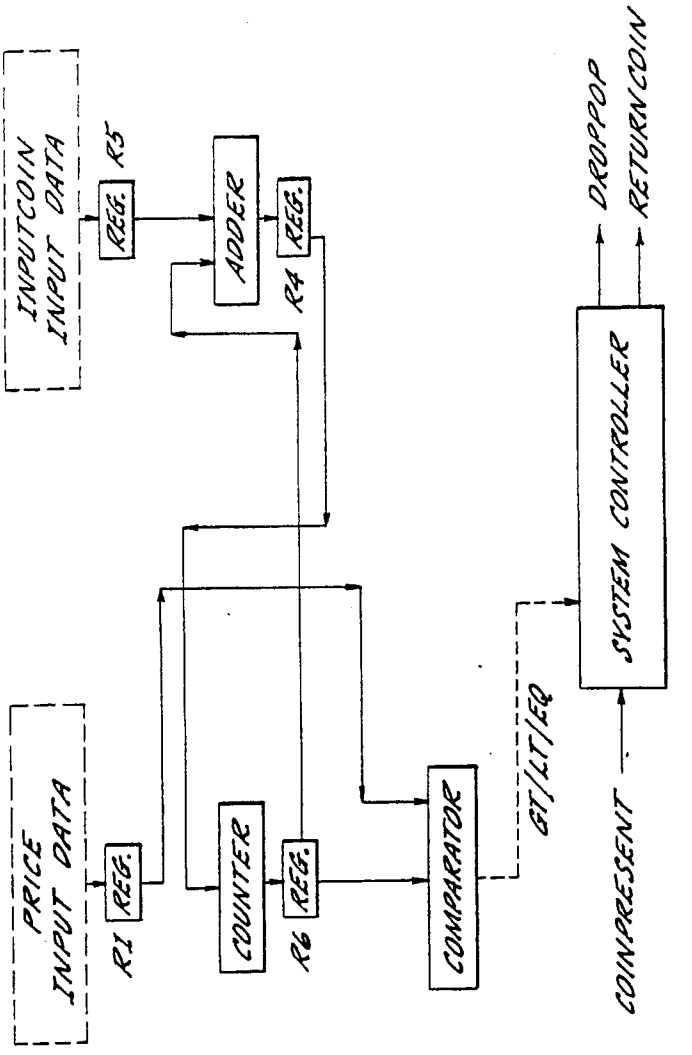

INPUTCOIN
INPUT DATA
REG.
R5
ADDER
REG.
R4
DROPPOP
RETURNCOIN
SYSTEM CONTROLLER
PRICE
INPUT DATA
REG.
R1
COUNTER
REG.
R6
COMPARATOR
GT/LT/EQ
COINPRESENT

Fig. 15.

KNOWLEDGE BASED METHOD AND APPARATUS FOR DESIGNING INTEGRATED CIRCUITS USING FUNCTIONAL SPECIFICATIONS

FIELD AND BACKGROUND OF THE INVENTION

This invention relates to the design of integrated circuits, and more particularly relates to a computer-aided method and apparatus for designing integrated circuits.

An application specific integrated circuit (ASIC) is an integrated circuit chip designed to perform a specific function, as distinguished from standard, general purpose integrated circuit chips, such as microprocessors, memory chips, etc. A highly skilled design engineer having specialized knowledge in VLSI circuit design is ordinarily required to design a ASIC. In the design process, the VLSI design engineer will consider the particular objectives to be accomplished and tasks to be performed by the integrated circuit and will create structural level design specifications which define the various hardware components required to perform the desired function, as well as the interconnection requirements between these components. A system controller must also be designed for synchronizing the operations of these components. This requires an extensive and all encompassing knowledge of the various hardware components required to achieve the desired objectives, as well as their interconnection requirements, signal level compatibility, timing compatibility, physical layout, etc. At each design step, the designer must do tedious analysis. The design specifications created by the VLSI design engineer may, for example, be in the form of circuit schematics, parameters or specialized hardware description languages (HDLs).

From the structural level design specifications, the description of the hardware components and interconnections is converted to a physical chip layout level description which describes the actual topological characteristics of the integrated circuit chip. This physical chip layout level description provides the mask data needed for fabricating the chip.

Due to the tremendous advances in very large scale integration (VLSI) technology, highly complex circuit systems are being built on a single chip. With their complexity and the demand to design custom chips at a faster rate, in large quantities, and for an ever increasing number of specific applications, computer-aided design (CAD) techniques need to be used. CAD techniques have been used with success in design and verification of integrated circuits, at both the structural level and at the physical layout level. For example, CAD systems have been developed for assisting in converting VLSI structural level descriptions of integrated circuits into the physical layout level topological mask data required for actually producing the chip. Although the presently available computer-aided design systems greatly facilitate the design process, the current practice still requires highly skilled VLSI design engineers to create the necessary structural level hardware descriptions.

There is only a small number of VLSI designers who possess the highly specialized skills needed to create structural level integrated circuit hardware descriptions. Even with the assistance of available VLSI CAD tools, the design process is time consuming and the probability of error is also high because of human involvements. There is a very significant need for a better and more cost effective way to design custom integrated circuits.

SUMMARY OF THE INVENTION

In accordance with the present invention a CAD (computer-aided design) system and method is provided which enables a user to define the functional requirements for a desired target integrated circuit, using an easily understood functional architecture independent level representation, and which generates therefrom the detailed information needed for directly producing an application specific integrated circuit (ASIC) to carry out those specific functions. Thus, the present invention, for the first time, opens the possibility for the design and production of ASICs by designers, engineers and technicians who may not possess the specialized expert knowledge of a highly skilled VLSI design engineer.

The functional architecture independent specifications of the desired ASIC can be defined in a suitable manner, such as in list form or preferably in a flowchart format. The flowchart is a highly effective means of describing a sequence of logical operations, and is well understood by software and hardware designers of varying levels of expertise and training. From the flowchart (or other functional specifications), the system and method of the present invention translates the functional architecture independent specifications into structural an architecture specific level definition of an integrated circuit, which can be used directly to produce the ASIC. The structural level definition includes a list of the integrated circuit hardware cells needed to achieve the functional specifications. These cells are selected from a cell library of previously designed hardware cells of various functions and technical specifications. The system also generates data paths among the selected hardware cells. In addition, the present invention generates a system controller and control paths for the selected integrated circuit hardware cells. The list of hardware cells and their interconnection requirements may be represented in the form of a netlist. From the netlist it is possible using either known manual techniques or existing VLSI CAD layout systems to generate the detailed chip level geometrical information (e.g. mask data) required to produce the particular application specific integrated circuit in chip form.

The preferred embodiment of the system and method of the present invention which is described more fully hereinafter is referred to as a Knowledge Based Silicon Compiler (KBSC). The KBSC is an ASIC design methodology based upon artificial intelligence and expert systems technology. The user interface of KBSC is a flowchart editor which allows the designer to represent VLSI systems in the form of a flowchart. The KBSC utilizes a knowledge based expert system, with a knowledge base extracted from expert ASIC designers with a high level of expertise in VLSI design to generate from the flowchart a netlist which describes the selected hardware cells and their interconnection requirements.

BRIEF DESCRIPTION OF THE DRAWINGS

The invention will be better understood by reference to the detailed description which follows, taken in connection with the accompanying drawings, in which

FIG. 1*a* illustrates a functional level design representation of a portion of a desired target circuit, shown in the form of a flowchart;

FIG. 1*b* illustrates a structural level design representation of an integrated circuit;

FIG. 1*c* illustrates a design representation of a circuit at a physical layout level, such as would be utilized in the fabrication of an integrated circuit chip;

FIG. 2 is a block schematic diagram showing how integrated circuit mask data is created from flowchart descriptions by the KBSC system of the present invention;

FIG. 3 is a somewhat more detailed schematic illustration showing the primary components of the KBSC system;

FIG. 4 is a schematic illustration showing how the ASIC design system of the present invention draws upon selected predefined integrated circuit hardware cells from a cell library;

FIG. 5 is an example flowchart defining a sequence of functional operations to be performed by an integrated circuit;

FIG. 6 is a structural representation showing the hardware blocks and interconnection requirements for the integrated circuit defined in FIG. 5;

FIG. 7 is an illustration of the flowchart editor window;

FIG. 8 is an illustration of the flowchart simulator window;

FIG. 9 is an illustration of the steps involved in cell list generation;

FIG. 10 is an example flowchart for a vending machine system;

FIG. 11 illustrates the hardware components which correspond to each of the three macros used in the flowchart of FIG. 10;

FIG. 12 is an initial block diagram showing the hardware components for an integrated circuit as defined in the flowchart of FIG. 10;

FIG. 13 is a block diagram corresponding to FIG. 12 showing the interconnections between blocks;

FIG. 14 is a block diagram corresponding to FIG. 13 after register optimization; and

FIG. 15 is a block diagram corresponding to FIG. 14 after further optimization.

DETAILED DESCRIPTION OF ILLUSTRATIVE EMBODIMENTS

FIGS. 1*a*, 1*b* and 1*c* illustrate three different levels of representing the design of an integrated circuit. FIG. 1*a* shows a functional (or behavioral) representation architecture independent in the form of a flowchart. A flowchart is a graphic representation of an algorithm and consists of two kinds of blocks or states, namely actions and conditions (decisions). Actions are conventionally represented in the flowchart by a rectangle or box, and conditions are represented by a diamond. Transitions between actions and conditions are represented by lines with arrows. FIG. 1*b* illustrates a structural (or logic) level representation of an integrated circuit. In this representation, blocks are used to represent integrated architecture specific circuit hardware components for performing various functions, and the lines interconnecting the blocks represent paths for the flow of data or control signals between the blocks. The blocks may, for example, represent hardware components such as adders, comparators, registers, system controllers, etc. FIG. 1*c* illustrates a physical layout level representation of an integrated circuit design, which provides the detailed mask data necessary to actually manufacture the devices and conductors which together comprise integrated circuit.

As noted earlier, the design of an integrated circuit at the structural level requires a design engineer with highly specialized skills and expertise in VLSI design. In the KBSC system of the present invention, however, integrated circuits can be designed at a functional level because the expertise in VLSI design is provided and applied by the invention. Allowing the designer to work with flowcharts instead of logic circuit schematics simplifies the task of designing custom integrated circuits, making it quicker, less expensive and more reliable. The designer deals with an algorithm using simple flowcharts at an architecture independent functional (behavioral) level, and needs to know only the necessary logical steps to complete a task, rather than the specific means for accomplishing the task. Designing with flowcharts requires less work in testing because flowcharts allow the designer to work much closer to the algorithm. On the other hand, previously existing VLSI design tools require the designer to represent an algorithm with complex circuit schematics at a structural level, therefore requiring more work in testing. Circuit schematics make it harder for the designer to cope with the algorithm function which needs to be incorporated into the target design because they intermix the hardware and functional considerations. Using flowcharts to design custom integrated circuits will allow a large number of system designers to access VLSI technology, where previously only a small number of designers had the knowledge and skills to create the necessary structural level hardware descriptions.

The overall system flow is illustrated in FIG. 2. The user enters the functional specifications of the circuit into the knowledge based silicon compiler (KBSC) **10** in the form of a flowchart **11**. The KBSC **10** then generates a netlist **15** from the flowchart. The netlist **15** includes a custom generated system controller, all other hardware cells required to implement the necessary operations, and interconnection information for connecting the hardware cells and the system controller. The netlist can be used as input to any existing VLSI layout and routing tool **16** to create mask data **18** for geometrical layout.

System Overview

The primary elements or modules which comprise the KBSC system are shown in FIG. 3. In the embodiment illustrated and described herein, these elements or modules are in the form of software programs, although persons skilled in the appropriate art will recognize that these elements can easily be embodied in other forms, such as in hardware.

Referring more particularly to FIG. 3, it will be seen that the KBSC system **10** includes a program **20** called EDSIM, which comprises a flowchart editor **21** for creating and editing flowcharts and a flowchart simulator **22** for simulation and verification of flowcharts. Actions to be performed by each of the rectangles represented in the flowchart are selected from a macro library **23**. A program **30** called PSCS (path synthesizer and cell selector) includes a data and control path synthesizer module **31**, which is a knowledge based system for data and control path synthesis. PSCS also includes a cell selector **32** for selecting the cells required for system design. The cell selector **32** selects from a cell

library 34 of previously designed hardware cells the appropriate cell or cells required to perform each action and condition represented in the flowchart. A controller generator 33 generates a custom designed system controller for controlling the operations of the other hardware cells. The knowledge base 35 contains ASIC design expert knowledge required for data path synthesis and cell selection. Thus, with a functional flowchart input, PSCS generates a system controller, selects all other hardware cells, generates data and control paths, and generates a netlist describing all of this design information.

The KBSC system employs a hierarchal cell selection ASIC design approach, as is illustrated in FIG. 4. Rather than generating every required hardware cell from scratch, the system draws upon a cell library 34 of previously designed, tested and proven hardware cells of various types and of various functional capabilities with a given type. The macro library 23 contains a set of macros defining various actions which can be specified in the flowchart. For each macro function in the macro library 23 there may be several hardware cells in the cell library 34 of differing geometry and characteristics capable of performing the specified function. Using a rule based expert system with a knowledge base 35 extracted from expert ASIC designers, the KBSC system selects from the cell library 34 the optimum cell for carrying out the desired function.

Referring again to FIG. 3, the cells selected by the cell selector 32, the controller information generated by the controller generator 33 and the data and control paths generated by the data/control path synthesizer 31 are all utilized by the PSCS program 30 to generate the netlist 15. The netlist is a list which identifies each block in the circuit and the interconnections between the respective inputs and outputs of each block. The netlist provides all the necessary information required to produce the integrated circuit. Computer-aided design systems for cell placement and routing are commercially available which will receive netlist data as input and will lay out the respective cells in the chip, generate the necessary routing, and produce mask data which can be directly used by a chip foundry in the fabrication of integrated circuits.

System Requirements

The KBSC system can be operated on a suitable programed general purpose digital computer. By way of example, one embodiment of the system is operated in a work station environment such as Sun3 and VAXStation-II/GPX Running UNIX Operating System and X Window Manager. The work station requires a minimum of 8 megabytes of main storage and 20 megabytes of hard disk space. The monitor used is a color screen with 8-bit planes. The software uses C programming language and INGRES relational data base.

The human interface is mainly done by the use of pop up menus, buttons, and a special purpose command language. The permanent data of the integrated circuit design are stored in the data base for easy retrieval and update. Main memory stores the next data temporarily, executable code, design data (flowchart, logic, etc.), data base (cell library), and knowledge base. The CPU performs the main tasks of creating and simulating flowcharts and the automatic synthesis of the design.

Flowchart Example

To describe the mapping of a flowchart to a netlist, consider an example flowchart shown in FIG. 5, which is of part of a larger overall system. In this illustrative flowchart, two variables, VAL1 and VAL2 are compared and if they are equal, they are added together. In this instance, the first action (Action 1) involves moving the value of variable VALI to register A. The second action comprises moving the value of variable VAL2 to register B. Condition 1 comprises comparing the values in registers A and B. Action 3 comprises adding the values of registers A and B and storing the result in register C.

In producing an integrated circuit to carry out the function defined in FIG. 5, the KBSC maps the flowchart description of the behavior of the system to interconnection requirements between hardware cells. The hardware cells are controlled by a system controller which generates all control signals. There are two types of variables involved in a system controller:

(1) Input variables: These are generated by hardware cells, and/or are external input to the controller. These correspond to conditions in the flowchart.

(2) Output variables: These are generated by the system controller and correspond to actions in the flowchart.

FIG. 6 illustrates the results of mapping the flowchart of FIG. 5 onto hardware cells. The actions and the conditions in the flowchart are used for cell selection and data and control path synthesis. The VALI register and VAL2 register and the data paths leading therefrom have already been allocated in actions occurring before Action 1 in our example. Action 1 causes generation of the data register A. Similarly, Action 2 causes the allocation of data register B. The comparator is allocated as a result of the comparison operation in Condition 1. The comparison operation is accomplished by (1) selecting a comparator cell, (2) mapping the inputs of the comparator cell to registers A and B, (3) generating data paths to connect the comparator with the registers A and B and (4) generating input variables corresponding to equal to, greater than, and less than for the system controller. Similarly the add operation in Action 3 causes selection of the adder cell, mapping of the adder parameters to the registers and creating the data paths.

Following this methodology, a block list can be generated for a given flowchart. This block list consists of a system controller and as many other blocks as may be required for performing the necessary operations. The blocks are connected with data paths, and the blocks are controlled by the system controller through control paths. These blocks can be mapped to the cells selected from a cell library to produce a cell list.

Interactive Flowchart Editor and Simulator

The creation and verification of the flowchart is the first step in the VLSI design methodology. The translation from an algorithm to an equivalent flowchart is performed with the Flowchart Editor 21 (FIG. 3). The verification of the edited flowchart is performed by the Flowchart Simulator 22 The Flowchart Editor and Simulator are integrated into one working environment for interactive flowchart editing, with a designer friendly interface.

EDSIM is the program which contains the Flowchart Editor 21 and the Flowchart Simulator 22. It also provides functions such as loading and saving flow-

charts. EDSIM will generate an intermediate file, called a statelist, for each flowchart. This file is then used by the PSCS program **30** to generate a netlist.

Flowchart Editor

The Flowchart Editor **21** is a software module used for displaying, creating, and editing the flowchart. This module is controlled through the flowchart editing window illustrated in FIG. 7. Along with editing functions the Flowchart Editor also provides checking of design errors.

The following is a description of the operations of the Flowchart Editor. The main editing functions include, create, edit, and delete states, conditions, and transitions. The create operation allows the designer to add a new state, condition, or transitions to a flowchart. Edit allows the designer to change the position of a state, condition or transition, and delete allows the designer to remove a state, condition or transition from the current flowchart. States which contain actions are represented by boxes, conditions are represented by diamonds, and transitions are represented by lines with arrows showing the direction of the transition.

Edit actions allows the designer to assign actions to each box. These actions are made up of macro names and arguments. An example of arguments is the setting and clearing of external signals. A list of basic macros available in the macro library **23** is shown in Table 1.

TABLE 1

Macro	Description
ADD (A,B,C)	C = A + B
SUB (A,B,C)	C = A − B
MULT (A,B,C)	C = A * B
DIV (A,B,C)	C = A div B
DECR (A)	A = A − 1
INCR (A)	A = A + 1
CLR (A)	A = 0
REG (A,B)	B = A
CMP (A,B)	Compare A to B and set EQ,LT,GT signals
CMP0 (A)	Compare A to 0 and set EQ,LT,GT signals
NEGATE (A)	A = NOT (A)
MOD (A,B,C)	C = A Modulus B
POW (A,B,C)	C = A B
DC2 (A,S1,S2,S3,S4)	Decode A into S1,S2,S3,S4
EC2 (S1,S2,S3,S4,A)	Encode S1,S2,S3,S4 into A
MOVE (A,B)	B = A
CALL sub-flowchart (A,B, . . .)	Call a sub-flowchart. Pass A,B . . .
START (A,B, . . .)	Beginning state of a sub-flowchart
STOP (A,B . . .)	Ending state of a sub-flowchart

The Flowchart Editor also provides a graphical display of the flowchart as the Flowchart Simulator simulates the flowchart. This graphical display consists of boxes, diamonds, and lines as shown in FIG. 7. All are drawn on the screen and look like a traditional flowchart. By displaying the flowchart on the screen during simulation it allows the designer to design and verify the flowchart at the same time.

Flowchart Simulator

The Flowchart Simulator **22** is a software module used for simulating flowcharts. This module is controlled through the simulator window illustrated in FIG. 8. The Flowchart Simulator simulates the transitions between states and conditions in a flowchart. The following is a list of the operations of the Flowchart Simulator:

edit data—Change the value of a register or memory.
set state—Set the next state to be simulated.
set detail or summary display—Display summary or detail information during simulation.
set breaks—Set a breakpoint.
clear breaks—Clear all breakpoints.
show breaks—Display current breakpoints.
step—Step through one transition.
execute—Execute the flowchart.
stop—Stop executing of the flowchart. history ON or history OFF—Set history recording on or off.
cancel—Cancel current operation.
help—Display help screen.
close—Close the simulator window.

The results of the simulation are displayed within the simulator window. Also the editor window will track the flowchart as it is being simulated. This tracking of the flowchart makes it easy to edit the flowchart when an error is found.

Cell Selection

The Cell Selector **32** is a knowledge based system for selecting a set of optimum cells from the cell library **34** to implement a VLSI system. The selection is based on functional descriptions in the flowchart, as specified by the macros assigned to each action represented in the flowchart. The cells selected for implementing a VLSI system depend on factors such as cell function, fabrication technology used, power limitations, time delays etc. The cell selector uses a knowledge base extracted from VLSI design experts to make the cell selection.

To design a VLSI system from a flowchart description of a user application, it is necessary to match the functions in a flowchart with cells from a cell library. This mapping needs the use of artificial intelligence techniques because the cell selection process is complicated and is done on the basis of a number of design parameters and constraints. The concept used for cell selection is analogous to that used in software compilation. In software compilation a number of subroutines are linked from libraries. In the design of VLSI systems, a functional macro can be mapped to library cell.

FIG. **4** illustrates the concept of hierarchical cell selection. The cell selection process is performed in two steps:

(1) selection of functional macros
(2) selection of geometrical cells

A set of basic macros is shown in Table 1. A macro corresponds to an action in the flowchart. As an example, consider the operation of adding A and B and storing the result in C. This function is mapped to the addition macro ADD(X, Y, Z). The flowchart editor and flowchart simulator are used to draw the rectangles, diamonds and lines of the flowchart, to assign a macro selected from the macro library **23** to each action represented in the flowchart, and to verify the functions in flowcharts. The flowchart is converted into an intermediate form (statelist) and input to the Cell Selector.

The Cell Selector uses a rule based expert system to select the appropriate cell or cells to perform each action. If the cell library has a number of cells with different geometries for performing the operation specified by the macro, then an appropriate cell can be selected on the basis of factors such as cell function, process technology used, time delay, power consumption, etc.

The knowledge base of Cell Selector **32** contains information (rules) relating to:

(1) selection of macros
(2) merging two macros

(3) mapping of macros to cells
(4) merging two cells
(5) error diagnostics

The above information is stored in the knowledge base **35** as rules.

Cell List Generation

FIG. **9** shows the cell list generation steps. The first step of cell list generation is the transformation of the flowchart description into a structure that can be used by the Cell Selector. This structure is called the statelist. The blocklist is generated from the statelist by the inference engine. The blocklist contains a list of the functional blocks to be used in the integrated circuit. Rules of the following type are applied during this stage.

map arguments to data paths
map actions to macros
connect these blocks

Rules also provide for optimization and error diagnostics at this level.

The cell selector maps the blocks to cells selected from the cell library **34**. It selects an optimum cell for a block. This involves the formulation of rules for selecting appropriate cells from the cell library. Four types of information are stored for each cell. These are:

(1) functional level information: description of the cell at the register transfer level.

(2) logic level information: description in terms of flip-flops and gates.

(3) circuit level information: description at the transistor level.

(4) Layout level information: geometrical mask level specification.

The attributes of a cell are:

cell name
description
function
width
height
status
technology
minimum delay
typical delay
maximum delay
power
file
designer
date
comment
inspector

In the cell selection process, the above information can be used. Some parameters that can be used to map macros to cells are:

(1) name of macro
(2) function to be performed
(3) complexity of the chip
(4) fabrication technology
(5) delay time allowed
(6) power consumption
(7) bit size of macro data paths

Netlist Generation

The netlist is generated after the cells have been selected by PSCS. PSCS also uses the macro definitions for connecting the cell terminals to other cells. PSCS uses the state-to-state transition information from an intermediate form representation of a flowchart (i.e. the statelist) to generate a netlist. PSCS contains the following knowledge for netlist generation:

(1) Data path synthesis
(2) Data path optimization
(3) Macro definitions
(4) Cell library
(5) Error detection and correction

The above information is stored in the knowledge base **35** as rules. Knowledge engineers help in the formulation of these rules from ASIC design experts. The macro library **23** and the cell library **34** are stored in a database of KBSC.

A number of operations are performed by PSCS. The following is a top level description of PSCS operations:

(1) Read the flowchart intermediate file and build a statelist.
(2) current_context=START
(3) Start the inference engine and load the current context rules.
(4) Perform one of the following operations depending upon current_context:
(a) Modify the statelist for correct implementation.
(b) Create blocklist, macrolist and data paths.
(c) Optimize blocklist and datapath list and perform error checks.
(d) Convert blocks to cells.
(e) Optimize cell list and perform error checks.
(f) Generate netlist.
(g) Optimize netlist and perform error checks and upon completion Goto 7.
(5) If current_context has changed, load new context rules.
(6) Goto **4**.
(7) Output netlist file and stf files and Stop.

In the following sections, operations mentioned in step 4 are described. The Rule Language and PSCS display are also described.

Rule Language

The rule language of PSCS is designed to be declarative and to facilitate rule editing. In order to make the expert understand the structure of the knowledge base, the rule language provides means for knowledge representation. This will enable the format of data structures to be stated in the rule base, which will enable the expert to refer to them and understand the various structures used by the system. For example, the expert can analyze the structure of wire and determine its components. The expert can then refer these components into rules. If a new object has to be defined, then the expert can declare a new structure and modify some existing structure to link to this new structure. In this way, the growth of the data structures can be visualized better by the expert. This in turn helps the designer to update and append rules.

The following features are included in the rule language:

(i) Knowledge representation in the form of a record structure.
(ii) Conditional expressions in the antecedent of a rule.
(iii) Facility to create and destroy structure in rule actions.
(iv) The assignment statement in the action of a rule.
(v) Facility for input and output in rule actions.
(vi) Provide facility to invoke C functions from rule actions.

The rule format to be used is as follows:

The rule format to be used is as follows:

Rule	<number> <context>	
If {		
	<if-clause>	
}		
Then	{	
	<then-clause>	
}		
where	<number>	rule number
	<context>	context in which this rule is active
	<if-clause>	the condition part of the rule
	<then-clause>	the action part of the rule

Inference Strategy

The inference strategy is based on a fast pattern matching algorithm. The rules are stored in a network and the requirement to iterate through the rules is avoided. This speeds up the execution. The conflict resolution strategy to be used is based on the following:

(1) The rule containing the most recent data is selected.

(2) The rule which has the most complex condition is selected.

(3) The rule declared first is selected.

Rule Editor

PSCS provides an interactive rule editor which enables the expert to update the rule set. The rules are stored in a database so that editing capabilities of the database package can be used for rule editing. To perform this operation the expert needs to be familiar with the various knowledge structures and the inferencing process. If this is not possible, then the help of a knowledge engineer is needed.

PSCS provides a menu from which various options can be set. Mechanisms are provided for setting various debugging flags and display options, and for the overall control of PSCS.

Facility is provided to save and display the blocklist created by the user. The blocklist configuration created by the user can be saved in a file and later be printed with a plotter. Also the PSCS display can be reset to restart the display process.

PSCS Example Rules:

Rule	1	
	IF	no blocks exist
	THEN	generate a system controller.
Rule	2	
	IF	a state exists which has a macro AND this macro has not been mapped to a block
	THEN	find a corresponding macro in the library and generate a block for this macro.
Rule	3	
	IF	there is a transition between two states AND there are macros in these states using the same argument
	THEN	make a connection from a register corresponding to the first macro to another register corresponding to the second macro.
Rule	4	
	IF	a register has only a single connection from another register
	THEN	combine these registers into a single register.
Rule	5	
	IF	there are two comparators AND input data widths are of the same size AND one input of these is same AND the outputs of the comparators are used to perform the same operation.
	THEN	combine these comparators into a single comparator.
Rule	6	
	IF	there is a data without a register
	THEN	allocate a register for this data.
Rule	7	
	IF	all the blocks have been interconnected AND a block has a few terminals not connected
	THEN	remove the block and its terminals, or issue an error message.
Rule	8	
	IF	memory is to be used, but a block has not been created for it
	THEN	create a memory block with data, address, read and write data and control terminals.
Rule	9	
	IF	a register has a single connection to a counter
	THEN	combine the register and the counter; remove the register and its terminals.
Rule	10	
	IF	there are connections to a terminal of a block from many different blocks
	THEN	insert a multiplexor; remove the connections to the terminals and connect them to the input of the multiplexor; connect the output of the multiplexor to the input of the block.

Additional rules address the following points:

remove cell(s) that can be replaced by using the outputs of other cell(s)

reduce multiplexor trees

use fan-out from the cells, etc.

Soft Drink Vending Machine Controller Design Example

The following example illustrates how the previously described features of the present invention are employed in the design of an application specific integrated circuit (ASIC). In this illustrative example the ASIC is designed for use as a vending machine controller. The vending machine controller receives a signal each time a coin has been deposited in a coin receiver. The coin value is recorded and when coins totalling the correct amount are received, the controller generates a signal to dispense a soft drink. When coins totalling more than the cost of the soft drink are received, the controller dispenses change in the correct amount.

This vending machine controller example is patterned after a textbook example used in teaching digital system controller design. See Fletcher, William I., *An Engineering Approach to Digital Design*, Prentice-Hall, Inc., pp. 491-505. Reference may be made to this textbook example for a more complete explanation of this vending machine controller requirements, and for an understanding and appreciation of the complex design procedures prior to the present invention for designing the hardware components for a controller.

FIG. 10 illustrates a flowchart for the vending machine controller system. This flowchart would be entered into the KBSC system by the user through the flowchart editor. Briefly reviewing the flowchart, the controller receives a coin present signal when a coin is received in the coin receiver. State0 and cond0 define a waiting state awaiting deposit of a coin. The symbol CP represents "coin present" and the symbol !CP repre-

sents "coin not present". Statel and condI determine when the coin has cleared the coin receiver. At state20, after receipt of a coin, the macro instruction ADD3.1 (lc, cv, sum) instructs the system to add lc (last coin) and cv (coin value) and store the result as sum. The macro instruction associated with state21 moves the value in the register sum to cv. The macro CMP.1 at state22 compares the value of cv with PR (price of soft drink) and returns signals EQ, GT and LT. The condition cond2 tests the result of the compare operation CMP.1. If the result is "not greater than" (!GT.CMP.1), then the condition cond3 tests to see whether the result is "equal" (EQ.CMP.1). If the result is "not equal" (!EQ.CMP.1), then control is returned to state0 awaiting the deposit of another coin. If cond3 is EQ, then state4 generates a control signal to dispense a soft drink (droppop) and the macro instruction CLR.1(cv) resets cv to zero awaiting another customer.

If the total coins deposited exceed the price, then state30 produces the action "returncoin". Additionally, the macro DECR.1 (cv) reduces the value of cv by the amount of the returned coin. At state31 cv and PR are again compared. If cv is still greater than PR, then control passes to state30 for return of another coin. The condition cond5 tests whether the result of CMP.2 is EQ and will result in either dispensing a drink (droppop) true or branching to state0 awaiting deposit of another coin. The macros associated with the states shown in FIG. 10 correspond to those defined in Table 1 above and define the particular actions which are to be performed at the respective states.

Appendix A shows the intermediate file or "statelist" produced from the flowchart of FIG. 10. This statelist is produced as output from the EDSIM program 20 and is used as input to the PSCS program 30 (FIG. 3).

FIG. 11 illustrates for each of the macros used in the flowchart of FIG. 10, the corresponding hardware blocks. It will be seen that the comparison macro CMP (A,B) results in the generation of a register for storing value A, a register for storing value B, and a comparator block and also produces control paths to the system controller for the EQ, LT, and GT signals generated as a result of the comparison operation. The addition macro ADD (A,B,C) results in the generation of a register for each of the input values A and B, a register for the output value C, and in the generation of an adder block. The macro DECR (A) results in the generation of a counter block. The PSCS program 30 maps each of the macros used in the flowchart of FIG. 10 to the corresponding hardware components results in the generation of the hardware blocks shown in FIG. 12. In generating the illustrated blocks, the PSCS program 30 relied upon rules 1 and 2 of the above listed example rules.

FIG. 13 illustrates the interconnection of the block of FIG. 12 with data paths and control paths. Rule 3 was used by the data/control path synthesizer program 31 in mapping the data and control paths.

FIG. 14 shows the result of optimizing the circuit by applying rule 4 to eliminate redundant registers. As a result of application of this rule, the registers R2, R3, R7, R8, and R9 in FIG. 13 were removed. FIG. 15 shows the block diagram after further optimization in which redundant comparators are consolidated. This optimization is achieved in the PSCS program 30 by application of rule 5.

Having now defined the system controller block, the other necessary hardware blocks and the data and control paths for the integrated circuit, the PSCS program 30 now generates a netlist 15 defining these hardware components and their interconnection requirements. From this netlist the mask data for producing the integrated circuit can be directly produced using available VLSI CAD tools.

```
name rpop;
data path @ic<0:5>, cv<0:5>, sum<0:5>, @pr<0:5>;
{
state4 : state0;
state30 : state31;
state21 : state22;
state20 : state21;
state0 :. !cp state0;
state0 :. cp state1;
state1 :. cp state1;
state1 :. !cp state20;
state22 :. GT.CMP.1 state30;
state22 :. !GT.CMP.1*EQ.CMP.1 state4;
state22 :. !GT.CMP.1*!EQ.CMP.1 state0;
state31 :. GT.CMP.2 state30;
state31 :. !GT.CMP.2*EQ.CMP.2 state4;
state31 :. !GT.CMP.2*!EQ.CMP.2 state0;
state30 :: returncoin;
state30 :: DECR.1(cv);
state4 :: droppop;
state4 :: CLR.1(cv);
state31 :: CMP.2(cv,pr);
state22 :: CMP.1(cv,pr);
state21 :: MOVE.1(sum,cv);
state20 :: ADD3.1(ic,cv,sum);
}
```

That which I claimed is:

1. A computer-aided design system for designing an application specific integrated circuit directly from architecture independent functional specifications for the integrated circuit, comprising

a macro library defining a set of architecture independent operations comprised of actions and conditions;

input specification means operable by a user for defining architecture independent functional specifications for the integrated circuit, said functional specifications being comprised of a series of operations comprised of actions and conditions, said input specification means including means to permit the user to specify for each operation a macro selected from said macro library;

a cell library defining a set of available integrated circuit hardware cells for performing the available operations defined in said macro library;

cell selection means for selecting from said cell library for each macro specified by said input specification means, appropriate hardware cells for performing the operation defined by the specified macro, said cell selection means comprising an expert system including a knowledge base containing rules for. selecting hardware cells from said cell library and inference engine means for selecting appropriate hardware cells from said cell library in accordance with the rules of said knowledge base; and

netlist generator means cooperating with said cell selection means for generating as output from the system a netlist defining the hardware cells which are needed to achieve the functional requirements of the integrated circuit and the connections therebetween.

2. The system as defined in claim 1 wherein said input means comprises means specification for receiving user

input of a list defining the series of actions and conditions.

3. The system as defined in claim 1 additionally including mask data generator means for generating from said netlist the mask data required to produce an integrated circuit having the specified functional requirements.

4. The system as defined in claim 1 wherein said input means comprises flowchart editor means specification for creating a flowchart having elements representing said series of actions and conditions.

5. The system as defined in claim 4 additionally including flowchart simulator means for simulating the functions defined in the flowchart to enable the user to verify the operation of the integrated circuit.

6. The system as defined in claim 1 additionally including data path generator means cooperating with said cell selection means for generating data paths for the hardware cells selected by said cell selection means.

7. The system as defined in claim 6 wherein said data path generator means comprises a knowledge base containing rules for selecting data paths between hardware cells and inference engine means for selecting data paths between the hardware cells selected by said cell selection means in accordance with the rules of said knowledge base and the arguments of the specified macros.

8. The system as defined in claim 6 additionally including control generator means for generating a controller and control paths for the hardware cells selected by said cell selection means.

9. A computer-aided design system for designing an application specific integrated circuit directly from a flowchart defining architecture independent functional requirements of the integrated circuit comprising

a marco library defining a set of architecture independent operations comprised of actions and conditions;

flowchart editor means operable by a user for creating a flowchart having elements representing said architecture independent operations;

said flowchart editor means including macro specification means for permitting the user to specify for each operation represented in the flowchart a macro selected from said macro library;

a cell library defining a set of available integrated circuit hardware cells for performing the available operations defined in said macro library;

cell selection means for selecting form said cell library for each specified macro, appropriate hardware cells for performing the operation defined by the specified macro, said cell selection means comprising an expert system including a knowledge base containing rules for selecting hardware cells from said cell library and inference engine means for selecting appropriate hardware cells from said cell library in accordance with the rules of said knowledge base; and

data path generator means cooperating with said cell selection means for generating data paths for the hardware cells selected by said cell selector means, said data path generator means comprising a knowledge base containing rules for selecting data paths between hardware cells and inference engine means for selecting data paths between hardware cells selected by said cell selection means in accordance with the rules of said knowledge base and the arguments of the specified macros.

10. The system as defined in claim 9 additionally including control generator means for generating a controller and control paths for the hardware cells selected by said cell selection means.

11. A computer-aided design system for designing an application specific integrated circuit directly from a flowchart defining architecture independent functional requirements of the integrated circuit, comprising

flowchart editor means operable by a user for creating a flowchart having boxes representing architecture independent actions, diamonds representing architecture independent conditions, and lines with arrows representing transitions between actions and condition and including means for specifying for each box or diamond, a particular action or condition to be performed;

a cell library defining a set of available integrated circuit hardware cells for performing actions and conditions;

a knowledge base containing rules for selecting hardware cells from said cell library and for generating data and control paths for hardware cells; and

expert system means operable with said knowledge base for translating the flowchart defined by said flowchart editor means into a netlist defining the necessary hardware cells and data and control paths required in an integrated circuit having the specified functional requirements.

12. The system as defined in claim 11 including mask data generator means for generating from said netlist the mask data required to produce an integrated circuit having the specified functional requirements.

13. A computer-aided design process for designing an application specific integrated circuit which will perform a desired function comprising

storing a set of definitions of architecture independent actions and conditions;

storing data describing a set of available integrated circuit hardware cells for performing the actions and conditions defined in the stored set;

storing in an expert system knowledge base a set of rules for selecting hardware cells to perform the actions and conditions;

describing for a proposed application specific integrated circuit a series of architecture independent actions and conditions;

specifying for each described action and condition of the series one of said stored definitions which corresponds to the desired action or condition to be performed; and

selecting from said stored data for each of the specified definitions a corresponding integrated circuit hardware cell for performing the desired function of the application specific integrated circuit, said step of selecting a hardware cell comprising applying to the specified definition of the action or condition to be performed, a set of cell selection rules stored in said expert system knowledge base and generating for the selected integrated circuit hardware cells, a netlist defining the hardware cells which are needed to perform the desired function of the integrated circuit and the interconnection requirements therefor.

14. A process as defined in claim 13, including generating from the netlist the mask data required to produce an integrated circuit having the desired function.

15. A process as defined in claim 13 including the further step of generating data paths for the selected integrated circuit hardware cells.

16. A process as defined in claim 15 wherein said step of generating data paths comprises applying to the selected cells a set of data path rules stored in a knowledge base and generating the data paths therefrom.

17. A process as defined in claim 16 including the further step of generating control paths for the selected integrated circuit hardware cells.

18. A knowledge based design process for designing an application specific integrated circuit which will perform a desired function comprising

storing in a macro library a set of macros defining architecture independent actions and conditions;

storing in a cell library a set of available integrated circuit hardware cells for performing the actions and conditions;

storing in a knowledge base set of rules for selecting hardware cells from said cell library to perform the actions and conditions defined by the stored macros;

describing for a proposed application specific integrated circuit a flowchart comprised of elements representing a series of architecture independent actions and conditions which carry out the function to be performed by the integrated circuit;

specifying for each described action and condition of said series a macro selected from the macro library which corresponds to the action or condition; and

applying rules of said knowledge base to the specified macros to select from said cell library the hardware cells required for performing the desired function of the application specific integrated circuit and generating for the selected integrated circuit hardware cells, a netlist defining the hardware cells which are needed to perform the desired function of the integrated circuit and the interconnection requirements therefor.

19. A process as defined in claim 18 also including the steps of

storing in said knowledge base a set of rules for creating data paths between hardware cells, and

applying rules of said knowledge base to the specified means to create data paths for the selected hardware cells.

20. A process as defined in claim 19 also including the steps of generating a controller and generating control paths for the selected hardware cells.

* * * * *

UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

PATENT NO. : 4,922,432 Page 1 of 4

DATED : May 1, 1990

INVENTOR(S) : Hideaki Kobayashi, et al.

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

ON TITLE PAGE: under the section "References Cited" under "Other Publications":

"Verifying Compiled Silicon", by E. K. cheng, VLSI Design, Oct. 1984, pp. 1-4." should be -- "Verifying Compiled Silicon", by E. K. Cheng, VLSI Design, Oct. 1984, pp. 1-4." --.

"quality of Designs from An Automatic Logic Generator", by T. D. Friedman et al., IEEE 7th DA Conference, 1970, pp. 71-89." should be -- "Quality of Designs from An Automatic Logic Generator", by T. D. Friedman et al., IEEE 7th DA Conference, 1970, pp. 71-89. --.

"Trevillyan-Trickey, H., Flamel: *A High Level Hardward Compiler*, IEEE Transactions On Computer Aided Design, Mar. 1987, pp. 259-269." should be -- Trevillyan-Trickey, H., Flamel: *A High Level Hardware Compiler*, IEEE Transactions On Computer Aided Design, Mar. 1987, pp. 259-269. --.

In the abstract:

Every occurrence of "functional architecture independent" should be -- architecture independent functional --.

Column 1, line 19, "a" should be -- an --.

[redacted]

UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

PATENT NO. : 4,922,432

DATED : May 1, 1990

INVENTOR(S) : Hideaki Kobayashi, et al.

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Column 2, line 10, "functional architecture independent" should be -- architecture independent functional --.

Column 2, line 21, "functional architecture independent" should be -- architecture independent functional --.

Column 2, lines 29-30, "functional architecture independent" should be -- architecture independent functional --.

Column 2, line 31, "structural" should be after "specific".

Column 3, lines 51-52, "representation" should be after "architecture independent".

Column 3, lines 61-62, "integrated" should be after "specific".

Column 6, line 62, after "22" insert -- . --.

Column 7, line 43 (in Table 1), "C = A B" should be -- C = A^B --.

Column 8, line 9 should end with the word "flowchart" and "history" should begin on the next line.

UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

PATENT NO. : 4,922,432 Page 3 of 4

DATED : May 1, 1990

INVENTOR(S) : Hideaki Kobayashi, et al.

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Column 10, line 23, "data paths" should be -- datapaths --.

Column 10, line 68, delete "The rule format to be used is as follows:".

Column 12, line 54, "Enqineering" should be -- Engineering --.

Column 13, line 55, "block" should be -- blocks --.

In the Claims:

Column 14, line 68, before "means" (first occurrence) insert -- specification --; after "means" (second occurrence) delete "specification".

Column 15, line 9, before "means" (first occurrence) insert -- specification --; after "means" (second occurrence) delete "specification".

Column 15, line 35, after "circuit" insert -- , --.

Column 15, line 36, "marco" should be -- macro --.

Column 15, line 49, "form" should be -- from --.

UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

PATENT NO. : 4,922,432

DATED : May 1, 1990

INVENTOR(S) : Hideaki Kobayashi, et al.

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Column 16, line 14, "condition" should be
-- conditions --.

Column 17, line 19, after "base" insert -- a --.

Signed and Sealed this

Fourteenth Day of January, 1992

Attest:

Attesting Officer

HARRY F. MANBECK, JR.

Commissioner of Patents and Trademarks

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Attorneys for Ricoh Company, Ltd.

UNITED STATES DISTRICT COURT
NORTHERN DISTRICT OF CALIFORNIA

RICOH COMPANY, LTD.,

Plaintiff,

vs.

AEROFLEX ET AL,

Defendants.

CASE NO. CV 03-4669-MJJ (EMC)

Consolidated with

CASE NO. CV 03-2289

NOTICE OF MANUAL FILING

SYNOPSYS, INC.,

Plaintiff,

vs.

RICOH COMPANY, LTD.,

Defendants.

Please take notice that Plaintiff Ricoh Company, Ltd., is filing the following documents on this date in paper form only:

1. Ricoh's Opposition to Defendants' Motion for Partial Summary Judgment.
2. Deposition transcript of Edward Dwyer of February 3, 2004 (Exhibit 7 to the Declaration of Michael Weinstein in Support of Ricoh's Opposition to Defendants' Motion for Partial Summary Judgment).
3. Chip Synthesis Workshop – Lab Guide (Exhibit 14 to the Declaration of Michael Weinstein in Support of Ricoh's Opposition to Defendants' Motion for Partial Summary Judgment).

Because the above documents include and refer to materials produced in discovery and designated confidential by the ASIC Defendants and Synopsys, a request to file these documents under seal will be filed contemporaneously.

Dated: August 23, 2005

Respectfully submitted,

Ricoh Company, Ltd.

By: /s/ Kenneth W. Brothers

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Attorneys for Ricoh Company, Ltd.

PROOF OF SERVICE

CASE: *Ricoh Company, Ltd. v. Aeroflex Incorporated, et al.*
Synopsys, Inc. v. Ricoh Company, Ltd.

CASE NOS.: U.S. District Court, N.D. Cal., Nos. C03-4669 and C03-2289 MJJ

I am employed in the City and County of San Francisco, California. I am over the age of eighteen years and not a party to the within action; my business address is 177 Post Street, Suite 300, San Francisco, California 94108. On August 23, 2005, I served the following document(s):

Ricoh's Opposition to Motion for Partial Summary Judgment.

Deposition transcript of Edward Dwyer of February 3, 2004 (Exhibit 7 to the Declaration of Michael Weinstein in Support of Ricoh's Opposition to Defendants' Motion for Partial Summary Judgment).

Chip Synthesis Workshop - Lab Guide (Exhibit 14 to the Declaration of Michael Weinstein in Support of Ricoh's Opposition to Defendants' Motion for Partial Summary Judgment).

on the parties, through their attorneys of record, by sending true copies thereof as shown below for service as designated below:

By Electronic Mail: I caused such document(s) to be served via electronic mail (email) on the parties in this action by transmitting a true copy to the following email address(es):

ADDRESSEE	PARTY
Teresa M. Corbin, Esq. Jaclyn Fink, Esq. Howrey Simon Arnold & White LLP 525 Market Street, Suite 3600 San Francisco, CA 94105-2708 CorbinT@howrey.com finkj@howrey.com	Defendants

I declare under penalty of perjury under the laws of the State of California that the foregoing is true and correct. Executed this August 23, 2005, at San Francisco, California.

/s/
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Attorneys for Ricoh Company, Ltd.

UNITED STATES DISTRICT COURT
NORTHERN DISTRICT OF CALIFORNIA
SAN FRANCISCO DIVISION

RICOH COMPANY, LTD, Plaintiff, vs. AEROFLEX, INC. ET AL. Defendants.	)))))))))	Case No. C03-4669 (Judge Jenkins) DECLARATION OF DR. V. THOMAS RHYNE

DR. V. THOMAS RHYNE declares as follows:

1. I have been retained by Ricoh Company, Ltd. ("Ricoh") as a technical expert in the above-styled litigation. I am over the age of 21 and am competent to make this declaration. Based on my personal knowledge and information, I hereby declare to all the facts in this declaration.

2. I have studied, taught, and practiced electrical engineering for over forty years. I hold degrees from Mississippi State University (BSEE with Honors, 1962), the University of Virginia (MEE, 1964), and the Georgia Institute of Technology (Ph.D. in EE, 1967). I have been a registered Professional Engineer in the State of Texas since 1969. I am also a Registered Patent Agent.

3. I taught electrical engineering, computer engineering, computer architecture, and computer science at the undergraduate and graduate levels full-time at Texas A&M University from 1967 to 1983 and part-time at the University of Texas from 1983 to 1990. My twenty-plus years of industrial experience includes work for the Electric Power Research Institute, Texas Instruments, Control Data Corporation, NASA, Texas Digital Systems, Inc. (a company I co-founded to produce microprocessor-based computer peripherals in 1976), the Microelectronics and Computer Technology Corporation (MCC), and Motorola, Inc.

4. I have extensive experience with computer technology and computer networking, including design, teaching, and use experience with a variety of computer systems, computer networks, and networking components. I have participated in the design of several computer systems and microprocessors, and have designed systems that made use of those devices as control elements. I am an experienced programmer in a variety

of programming languages as well as assembly-level language on a number of different computers and microprocessors. I have also chaired and otherwise participated in a number IEEE and ISO/IEC standards committees.

5. While at MCC, between 1983 and 1995, I was intimately involved in computer aided design (CAD) for large, complex integrated circuits and the use of expert systems technology in that area of application as well as other areas of application.

6. My experience and qualifications have been recognized by the Texas Society of Professional Engineers (Young Engineer of the Year in Texas, 1973), the American Society for Engineering Education (Terman Awardee as the "Outstanding Young Electrical Engineering Educator in the U.S.," 1980), the Institute of Electrical and Electronics Engineers (IEEE Fellow, 1990), and the Accreditation Board for Engineering and Technology (ABET Fellow, 1992). I am the author of thirty technical papers, have presented papers at thirty-seven conferences, and have authored an award winning textbook adopted at over thirty-five U.S. and international universities.

7. I have extensive experience with the accreditation of engineering and computer science programs in the U.S. and abroad, an activity which has provided me an excellent opportunity to become and remain familiar with the program curricula, faculties, and graduates from a large number of U.S. and international colleges and universities. I represented the IEEE for five years on the Engineering Accreditation Commission, and for six years on the Board of Directors of the Accreditation Board for Engineering and Technology (ABET). I also was appointed by the National Research Council to chair the Panel of Assessment for the Electronics and Electrical Engineering Laboratory of the

U.S. National Institute of Standards and technology. I served on that Panel for seven years.

8. I retired from full-time work in 1997, although I have worked part-time as a consulting engineer for the past thirty years, including work in the field of application-specific system design.

9. I have reviewed U.S. Patent No. 4,922,432 ("the '432 patent") and believe that it describes and claims an integral portion of the manufacturing process utilized in the semiconductor industry for the manufacture of application specific integrated circuit (ASIC) products.

10. From my own design work, and my experience and knowledge of the work of others in the field, I believe the following process steps are an essential part of the manufacture of ASIC products:

A. Describing a series of functions that are to be performed by the desired ASIC product to be manufactured.

B. Performing logic synthesis to identify the logic blocks needed to achieve the desired functionality.

C. Selecting the circuit components in a desired technology that are to be used to implement the synthesized logic blocks.

D. Producing a description of the circuit components as well as their respective connections in the form of a netlist.

E. Creating from the netlist a layout of the circuit components (and their interconnections) that fits within the area of the silicon die to be used for the ASIC product.

F. Formulating as mask data a complete representation of the integrated circuit

for fabrication on the silicon die.

G. Using the mask data to create the set of multiple masks required for producing the circuit layout on the silicon die to form the ASIC product.

11. Based on my personal knowledge and experience in the semiconductor industry, I believe that the process described and claimed in the '432 patent would be considered in the industry to be an essential portion of the synthesis-based manufacture of an ASIC product.

I declare under penalty of perjury under the laws of the United States of America that the foregoing is true and correct. Signed at Austin, TX on February 24, 2004.

V. Thomas Rhyne, Ph.D., P.E., R.P.A.

Integrated Circuit Manufacturing Synopsis

Michael Heynes, Ph.D.
Anne K. Miller

Published by:
Semiconductor Services
735 Hillcrest Way
Redwood City, California 94062-3428

ISBN number 1-887574-05-0
Third Edition 2002

immediately and no additional work, time or materials are invested in wafers which are unlikely to yield good die.

An important factor in managing a production line is predictability. Managers need to know the volume of product that can be produced in the future in order to plan shipments to customers and to anticipate capacity requirements which involve facilities, equipment and personnel.

Thus, considerable effort is expended in characterizing a production line in terms of expected yields correlated to various process parameters including defect levels. This is done to spot deviations quickly and rectify them before serious yield loss occurs. Statistical Process Control (SPC) is used for this and yield improvement purposes.

The IC design itself can be a problem. Some designs have little tolerance for unavoidable process variations. Product test and design engineers must often modify the design to achieve an acceptable yield.

V. Thomas Rhyne

April 14, 2004

Volume 1

Ricoh Company, LTD. v. Aeroflex Incorporated, et al

Condensed Transcript and Word Index
prepared by:

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UNITED STATES DISTRICT COURT
NORTHERN DISTRICT OF CALIFORNIA
SAN FRANCISCO DIVISION

RICOH COMPANY, LTD., Plaintiff,
VS.
AEROFLEX, INCORPORATED, AMI SEMICONDUCTOR, INC., MATROX ELECTRONIC SYSTEMS, LTD., MATROX GRAPHICS, INC., MATROX INTERNATIONAL CORP., and MATROX TECH, INC., Defendants.

Case No. CV 03-04669 MJJ (EMC)

****

ORAL DEPOSITION OF

V. THOMAS RHYNE

APRIL 14, 2004

****

ORAL DEPOSITION OF V. THOMAS RHYNE, produced as a witness at the instance of the Defendants, and duly sworn, was taken in the above-styled and numbered cause on the 14th of April, 2004, from 8:58 A.M. to 11:51 A.M., before Kathleen Casey Collins, CSR, in and for the State of Texas, reported by machine shorthand, at the Intercontinental Stephen F. Austin Hotel, 701 Congress Avenue, Stateboard Room, Austin, Travis County, Texas, pursuant to the Federal Rules of Civil Procedure.

APPEARANCES

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* * *

INDEX

* * *

EXHIBIT INDEX

* * *

V. THOMAS RHYNE,
having being first duly sworn, testified as follows:

EXAMINATION

BY MR. KELLEY:

Q. Good morning, Dr. Rhyne.

A. Good morning.

Q. Let me just start by getting what background do you have that you understand is -- that you think is relevant to the sort of subject matter of your -- Well, let me back up.

Am I correct in understanding that your -- that your Declaration talks about the semiconductor process?

A. That's one way to characterize it. I'm not sure it uses those terms.

Q. Well, let me get you to characterize it so that we can use those terms.

A. Why don't you give me a copy of it.

Q. Okay.

A. I think it pretty well speaks for itself.

MR. KELLEY: Let's mark this as Rhyne 1.

(Exhibit No. 1 marked)

MS. ALLEN: What's the question?

Q. In Paragraph 10, the first line says, "From my own design work, and my experience and knowledge of the work of others in the field, I believe the following process steps are an essential part of the manufacture of ASIC products."

So the question that I have is what background do you have that is relevant to the question of process steps involved in the manufacture of ASIC products?

A. Well, I attempted to set forth in the paragraphs primarily 2 through 8 where I've worked and what my experience has been. I think maybe if you want to ask me about specific areas within those portions of the Declaration, I can expand on it. But all of that work -- I guess I can't say all of it, but much of that work has related to the manufacture of ASICs.

Q. Okay. I guess we should take it step-by-step. Did you -- have you been involved -- have you been involved in a team that designed an ASIC that was then manufactured and produced at any point during your career?

A. Yes.

Q. Okay. And what -- In Paragraph 3, you call out several things from teaching to different positions you've held. Can you identify which of those positions involved ASIC design or manufacture?

A. Sure. I taught that subject at Texas A&M under the rubric I guess you'd say of VLSI design and computer-aided design.

Q. Okay.

A. I did ASIC design at Texas Instruments on two different occasions when I worked for them. And I was involved in ASIC design and manufacture at Motorola, which is

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the last one listed in Paragraph No. 3. I've worked on computer-aided design, working directly with participating companies who did ASIC design and actually manufactured ASICs, during the time I was at the Microelectronics and Computer Technology Corporation, as well. So pretty much a very high percentage of the work that was listed by company name in Paragraph 3.

Q. Okay. You mentioned manufacturing in connection with Motorola. Was there something about your job at Motorola that had an element relating to manufacture that was different than -- because you only mentioned it in connection with Texas Instruments? Did you get more heavily involved in the manufacturing of ASICs when you were at Motorola?

MS. ALLEN: Object; vague and compound.

A. I don't know that I separate those two parts in terms of the overall process of manufacture of an ASIC. But I was more closely aligned, while at Motorola, with the actual semiconductor part of the overall manufacturing process, the clean rooms and that part of that. That was part of my responsibility.

Q. Did Motorola have its own foundry when you were there?

A. Yeah. There were several that were running here in Austin. There were others in other places, but I was -- I was familiar with the ones here in Austin.

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Q. So you had some involvement with the foundries in Austin?

A. I did.

Q. All right. What was the year? What year are we talking about when you were at Motorola?

A. I joined Motorola in 1995 and was with them until almost '98. So it was about three years.

Q. Okay. And what was your position? What was your title at Motorola?

A. I think it's on my resume. I was in something called strategic technology, which -- and I don't remember the exact title --

Q. Okay.

A. -- but I believe it's on my resume.

MR. KELLEY: Do you have a copy of his resume so we could get that?

MS. ALLEN: We may have one in our files, but we should be able to get one.

MR. KELLEY: I'd appreciate it.

Q. (Mr. Kelley continuing) So you're not exactly sure what the title was, but it was something to do with strategic technology. What was that about?

A. Strategic technology dealt with any situation in which Motorola exchanged intellectual property with another technology department, and so it covered a lot of different

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aspects of that.

But one of the key things that I thought was relevant to your earlier question was there were a number of joint foundries that were operated by Motorola in conjunction with other partners; and I was involved in the management of those joint relationships, as well as the placement of some specific ASICs into those foundries for manufacture.

Q. Have you ever used -- Well, let be back up.

Are you familiar term with the term "logic synthesis" or "design synthesis"?

A. Yes.

Q. And are you familiar with the tools that are used for logic synthesis?

A. To some degree, yeah. I was probably much more familiar with them back in the 1980s and early '90s when I was there working in the CAD business, which I understand is a relevant time frame. But I am still -- I still keep up with that field to some degree.

Q. Okay. When you were at MCC, did you use any of those logic synthesis tools or --

A. Well, we were actually developing logic synthesis tools there. But I did use -- I used computer-aided design systems, which -- which worked through the design process. And I -- we did have some -- for example, the Berkeley tool set and some other things that included synthesis tools, and I

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had some experience with that.

Q. Okay. What other tool sets were you familiar with back at the time, whether you used them or not, that had some logic synthesis component?

A. We had on site the Mentor Graphics computer-aided design system. We had opportunities there to experiment with the Cadence design systems, which was sort of evolving. Cadence was formed during the time frame when I was at MCC.

And then there was a period when I worked with a computer-aided design frameworks -- framework standards laboratory at MCC, and that involved working with 20 or 25 of the computer-aided design companies and their products in a number of technology demonstration efforts that went on within that community.

Q. Do you remember what the name of the Cadence logic synthesis tool was?

A. No.

Q. Okay. But their -- But both Cadence and Mentor Graphics had a logic synthesis component to their CAD packages at that time?

A. I -- I can't tell you for sure whether they had something that today I would call a logic synthesis tool or not, and their tools were evolving over that almost 10 -- more than 10-year period when I was working with them. So I -- I can't tell you for sure whether the CAD system that we had for

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Mentor or the one version that I worked with from Cadence had a synthesis tool.

But there were synthesis tools around MCC. I had experience with them. And, as I said, we were attempting to develop synthesis tools ourselves. And then during that standards process, we had synthesis tools involved in the technology demonstration projects that I talked about. But I'm not sure I could name any particular name that was assigned to them.

Q. Were you -- What was your role then? You mentioned that MCC was trying to develop its own synthesis tools. What was your role in the synthesis tool product there?

A. Probably more as a manager than a direct technical contributor. I was aware that there were people who were looking at both logical and physical synthesis. I knew what their work was doing. I had oversight to that. And then I particularly directed the -- what came to be known as the framework effort that provided a number of enabling technologies for the synthesis tools that actually operate in a design mode.

Q. You mentioned this framework effort. Can you tell me -- You said this included enabling technologies for synthesis. How did -- Can you give me some more information about that?

A. Sure. Things like distributed design databases,

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human interfaces, graphics. We worked a lot on standard representations of critical design data.

Q. Am I correct in understanding these were things that could be used in the design process high level down to a lower level so that they could be used in synthesis, but they might also be relevant to a schematic design or a layout? Is that why it's called a framework or isn't it?

MS. ALLEN: Objection; compound, vague, ambiguous.

A. Well, framework was the terminology within the CAD industry for an attempt to provide a standard set of interfaces that would allow people trying to develop computer-aided design systems to pick and choose tools at various parts of the design process from different vendors so that they would not necessarily be trapped, say, into only the set of tools that Mentor offered or Cadence offered but, rather, could either use in-house developed tools or whatever at various stages of the overall design process to accomplish the different parts of that process without having to do a lot of interfacing work themselves.

Q. So you were -- you were trying to define some standard interfaces in the process below where people could change from one tool to a different manufacturer -- or sellers to different product lines, basically?

A. That's not a bad way of characterizing it. But I

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think the whole industry was talking about it. I'm not sure that the integrated CAD vendors particularly thought that was a good idea. But there was a major effort within the industry, and it was primarily coordinated by a laboratory that I set up at MCC. In fact, that effort has continued on today. So it's attempting to carry that concept forward.

Q. You mentioned -- A few questions ago, you mentioned logical synthesis and physical synthesis. Can you tell me what logical synthesis is and what physical synthesis?

A. Well, I think kind of --

MS. ALLEN: I just want to object as compound and vague.

A. I'll take your two questions in two pieces --

Q. That would be great.

A. -- and resolve the compound.

Q. Okay.

A. I think I recall. If I forget the second one, you can --

Q. Okay.

A. You asked about what I understood logic synthesis to mean, and I don't think that's a term that has a very precise meaning. But generally it involves moving from one representation within the design process to another representation where what you're dealing with is the logical blocks, if you will; and depending on what your style is,

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those blocks could be as simple as gates and flipflops or be as complicated as a complete and substantiated core processor.

Physical is where you move down the design and manufacturing hierarchy to the point where you actually -- the old phrase used to be pushing polygons - I don't know if you recall that - where you're -- you're beginning or maybe ending up by dealing with the physical characteristics of what will be produced in silicon and the methods of the manufacturing process.

Q. Okay. Going back here to the early '90s when you were at MCC, am I correct in understanding that at that time people were designing ASICs sometimes using synthesis tools and sometimes not?

A. Okay. Two --

MS. ALLEN: Objection; compound.

A. The first thing, I was at MCC, again, from the early '80s on through the early '90s, and so you misspoke a little bit --

Q. Okay.

A. -- and as I say, that was a very dynamic period in the development of design tools.

But the answer to your question is yes. People designed without using what I would call a synthesis tool; just a manual effort based on their own skills. It may be a whole team of people required to do that. But then throughout

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that period and subsequently, synthesis began to be more commonly used because better synthesis tools came to be available.

Q. And maybe you could just briefly explain how you would design ASICs without using synthesis.

MS. ALLEN: Objection. It's outside the scope of the Declaration.

A. I think the way I, or people who practice that art, would probably start in the early days with a schematic, make a logical schematic and translate that schematic then into maybe a transistor circuit schematic. There was a lot of ways to represent that. And then eventually move to a physical design process where they would lay out those transistors and their interconnections and then move on through to the mass development.

I think -- I think those are terms that probably are well understood in the art, and so I'm assuming those are understood by you.

Q. Okay. The patent talks about technology binding, I think. Is that a phrase you're familiar with?

A. I don't --

MS. ALLEN: Objection. It's outside the scope of the Declaration.

A. And I'm not prepared to really discuss the metes and bounds of what the patent may or may not say today. But what

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was the two words that you --

Q. Well, let me back up. Setting aside the patent -- I mean, I was just trying to use the terminology and it's not necessary. Are you familiar with the phrase "technology binding"?

MS. ALLEN: Again, objection. It's outside the scope of the Declaration. To the extent it's calling for an interpretation, I would invoke attorney/client privilege -- or work product privilege. Excuse me.

A. It's not a term that I think I've used commonly, but I think I can assign a meaning to it but --

MS. ALLEN: Well, let me -- let me ask this: Even though I think you may be impinging on things that might be attorney/client work product privilege, can we just have a sort of standing agreement if I don't instruct him not to answer that you're not going to use his answer as any claim of waiver or something like that?

MR. KELLEY: It is what it is. No, you're not going to get any agreement from me. If you want to tell him not to answer, you can tell him not to answer it. That decision is on your hands. I'm not going to agree to that.

MS. ALLEN: Well, I would just instruct you to the extent it's outside what you relied upon to opine in your Declaration that you not give any interpretation of --

MR. KELLEY: Well, I understand -- I'm sorry.

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But I understand your concern is that I'm trying to get into claim construction, and I'm not trying to do that.

Q. (Mr. Kelley continuing) So let me just -- let me just say my understanding of technology binding and you can agree or disagree or let's use this as a definition. Technology binding involves taking a logical function and saying this is the specific library cell or -- that I'm going to use to make that function and actually incorporating that information into the design.

MS. ALLEN: Again, I object. It's outside the scope of the Declaration.

Q. Do you understand what I'm talking about if we use that definition?

A. I think it's pretty vague. If you want to use that as a basis for further questioning, feel free. I'll try to understand it.

MS. ALLEN: You have no obligation to speculate.

Q. Well, the issue I'm trying to get at is here you were describing how people designed ASICs without using logical synthesis. All I'm trying to find out is when they -- when they did design without using synthesis, was one of the things they had to do is go in and say, "Well, I'm going to -- Here's my cells. Here's my technology options that are available to me. I'm going to implement this function using

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that cell or this function using that cell"?

MS. ALLEN: Objection; vague, compound.

A. I think in the design process that you tended to move through various representations of the product, and there were -- there are points at which you have to become -- well, where the representation becomes more specific as to some technology issue. There are a lot of different layers as to what that technology binding may be, and so that's why I say I think your definition is a little vague, but I'm not disagreeing with it. I'm just not accepting it as being truly characteristic -- characteristic of my understanding or my prior experience of how people designed absent synthesis.

Q. Okay. Well, let me ask you -- let me ask the question this way: In order to -- or what we're talking about now is design not using logic synthesis; and in order to do that, somehow the design had to be mapped into a target technology. Is that correct?

MS. ALLEN: Objection; compound and outside the scope of the Declaration.

A. I gather what -- when you're saying design without synthesis, I'm going to use the phrase "manual design" --

Q. That's fine with me.

A. -- computer-aided manual design. And my problem is I'm not sure what you mean by "technology," because there are different layers to the technology linkage during the

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manufacturing process. So I'm not sure what technology linkage you're talking about. It's not just a single point at which the technology affects you. There are multiple points.

Q. All right. Well, let's talk about this. What's the term -- What does the term "tapeout" mean?

A. In the industry, it is commonly used to mean the point at which -- it even dates back to the old magnetic tape. It's the point at which you had a tape that you could deliver in some ways to the next stage of the process of manufacturing the chip. But it generally applied to the point at which you had actually completely bounded down to the point where you were ready to pass it over to, say, a foundry, which would -- depending on the nature of what the -- what the representation on the tape was of the product, it could actually define the masks, or it could define enough about the physical device -- physical characteristics of the device that masks could then be made. I think there were different -- different rules of what would be on the so-called tape. But it's -- it's a late stage in the design and manufacturing process.

Q. Okay. So with regard -- backing up from -- from tapeout, how do I -- how do I get -- how do I produce this mask information or other information that's going to be on my tape?

A. I don't know. That question is too vague for me to know how to answer.

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Q. Okay. What is a netlist?

THE REPORTER: A what?

MR. KELLEY: Netlist, all one word.

A. A netlist is commonly understood to be a set of what's called building blocks or components I think is a term I used at a couple points here in my Declaration and the interconnections between them and -- and, also, the outside world, if you think about the boundaries of the device that's being produced in accordance with the representation of that netlist.

Q. Okay. Is one of the things that a designer might construct a netlist of library cells that are available using a certain technology that a foundry can implement?

A. That certainly would be a way of representing the device that's being designed and manufactured.

Q. Okay. Are there -- Let me back up. Let me start this again. Could then -- Could you then use that information to produce the tapeout information?

A. You could, yes.

Q. Okay. Are there other ways of getting the tapeout information?

MS. ALLEN: Objection; ambiguous. It's outside the scope of the Declaration.

A. I believe that there are.

Q. Okay. What are those?

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A. Well, the only other one that --

MS. ALLEN: Objection; outside the scope of the Declaration.

A. The only other thing that comes to mind is that there are physical representations of the physical layout that were used at some stages in the design, and there were ways to pass that physical layout, which is not exactly a netlist. It's a different representation but in a tapeout fashion. As I said earlier, it could also be mask. There are other ways to exchange mask information.

Q. Okay. How -- how would a designer typically get to physical layout? I presume they're not going to start -- they're not going to start the design by drawing geometries on a piece of paper. Is that correct?

A. Again, there's a hierarchy that developed over, you know, 20 years or so here. In the early days, people did exactly that; although, the level of complexity was limited, of course, by the ability to deal with the physical devices.

I mean, basically, throughout all of this hierarchy, people have started with some high level -- higher level representation for design and transformed it into another representation that was, in a sense, a lower level; and at some point, they began to impact the technologies that were going to eventually be used to manufacture the actual silicon. So they would just move from stage to stage, from

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representation to representation. The lower level representations would become more affected by the particular choices in technologies that were going to be used to build it at the end of the process.

Q. Okay. But those choices of technologies, throughout the '80s and '90s, people -- when some of the ASICs were being built, those choices were being made manually?

MS. ALLEN: Is that a question?

MR. KELLEY: It is a question.

Q. Is that true or not?

MS. ALLEN: Objection; compound and vague and outside the scope of the Declaration.

A. Yeah. You've got -- again, I don't know how -- I mean, my guess is they're probably still doing it manually today. Not everybody is using synthesis. But as long as we're talking about the manual process, then they would be making those bindings, if you will, or these changes in representation from stage to stage manually.

Q. Okay. Do you know what a mask house is?

A. I couldn't hear you.

Q. I'm sorry. Do you know what a mask house is?

A. I think I do.

Q. What do you -- what do you understand it to mean?

A. A company that makes masks for -- for use in the manufacture of integrated circuits.

Q. A mask house is separate from the foundry, or are they tied to the foundry, or is it a little bit of both?

A. My experience is it could be either way. Some foundries provide mask manufacture as part of their services. Others accept information or the actual masks as part of the foundry process. So I'm not aware that there's any set split between those two procedures.

Q. But one possible flow is you have these designers in an organization of one company, a mask house is a second company, and the foundry is a third and separate company. Is that correct?

MS. ALLEN: Objection; ambiguous and compound.

A. As best I understand the proposed organization, I think that could be the case. I couldn't necessarily give you a specific set of examples. I can neither confirm or deny that that's been -- that's been the practice.

Q. There -- am I correct that there are certainly companies that do not have their own foundry and have a separate third-party foundry -- a separate foundry to do their --

A. I believe --

Q. -- application?

A. I believe that's true.

Q. Okay. And those businesses could use a mask house separate from the foundry. Is that correct?

A. I believe --

MS. ALLEN: Objection; ambiguous.

A. Again, "mask house" is a term that you've come up with. I think that there are a variety of places that you can go to to have the next stage in the manufacturing process implemented; and by that stage, I mean going ahead and making the masks from the data that you've gotten to a certain point.

Again, I think of it, as I told you earlier, as a set of representations that you move through. There's a point at which a representation is the mask set itself. Somebody has to make that mask from whatever the prior representation is. I think you can contract with people to do that.

Q. Okay. Are the -- do you know are the engineers and the folks who do the mask making, are they the same people who do the design in logical synthesis, or are these a separate group of engineers typically?

MS. ALLEN: Objection; ambiguous and outside the scope of the Declaration.

A. I guess there probably are people who can carry the process from beginning to end, but I also think there are specialists at each stage of the process that know how to do that as an art and provide that art to the overall process.

Q. Do you know which -- which arrangement is more common, that somebody could do all of it from the high level

end of the design spec all of the way down to doing the mask making themselves or contracting?

A. Well, given the complexities of the processes that are used today and the nature of the kinds of masks today, and I'm not really prepared to opine on this in any detail back in the '80s, I think it would be unlikely that a single individual would have the skillset to go from -- from the top all of the way down through the manufacture of the mask.

Q. Okay.

A. It's a very complicated art today and was becoming even more complicated during the time frame I was working at MCC and Motorola.

MR. KELLEY: Let me mark this as Rhyne No. 2.

(Exhibit No. 2 marked)

Q. I'm interested in the second and third page in this document.

A. Could you tell me what --

MS. ALLEN: Yeah. Objection to this exhibit. It's outside the scope of the Declaration.

A. Could you tell me what this exhibit is?

Q. Well, it's a flowchart. If you'll look at Page 2 and 3, you will --

A. Where did it come from? Is it attorney developed or --

Q. No. I'm just going to show you it. I just want you

to look at the typical chip design flow on here and tell me if this -- just take a look at it, and I'm going to want to talk about some of the terms on it. You don't have to adopt it as a design flow or your understanding as a design flow, but I want -- I want to talk about whether -- what some of these terms mean, and I want your understanding of how a typical chip design flow works, if it's similar to this, or what some of these terms mean. Tell me when you've had a chance to look at it.

MS. ALLEN: And I object to this as outside the scope of the Declaration.

A. Do you have a time frame for this? I don't know -- I think I've heard of the EDA Consortium, but I don't know what time frame this is. I see a "99." Can you give me a feel for when this was developed?

Q. The answer to your question is no, I'm not familiar with when it was developed.

A. So it could be anywhere from 1950 to 2004?

Q. It could be; although, I see there's some products here that probably didn't exist in 1950.

A. Well, go ahead and ask your questions. I'll just note for the record that I haven't seen this before, and I may or may not be able to provide you any cogent input to your questions.

Q. Sure. What I want to find out is if you've -- do

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you see that there's sort of a organized nine different -- they've identified nine different steps. And, obviously, any process can be broken down into a number of pieces. But I wanted to know if you've heard of the term "physical verification" before?

A. Well, first off, I don't --

MS. ALLEN: Objection --

THE WITNESS: I'm sorry. Go ahead, Ms. Allen.

MS. ALLEN: I just want to object to the representation of the exhibit. But go ahead and answer the question.

A. You threw me when you said nine steps. I didn't understand that.

Q. I see 10. You're right.

MS. ALLEN: I still object to the representation of the exhibit, but go ahead.

A. So reask your question.

Q. Sure. Have you heard of the phrase "physical verification" before?

A. Yes.

Q. Okay. And what is it? What is physical verification?

MS. ALLEN: I object. It's outside the scope of the Declaration.

MR. KELLEY: You know, I'm just going to

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address that briefly. His Declaration is about process flow, the EDA process and what's required, and "logic design/synthesis" is right up there on the left side, and he's saying that this is part of manufacturing. So it seems to me that the EDA process is directly involved in his Declaration.

Now, I just wanted to state that for the record. You can agree or disagree. It doesn't seem to me that it's outside the scope of his Declaration at all.

MS. ALLEN: I object to the exhibit as being outside the scope of the Declaration. Clearly we don't agree but --

MR. KELLEY: Go ahead and say it.

A. I don't recall your question before the colloquy.

Q. The question was what is physical verification?

A. I do recall that. Well, as -- as whomever made this hierarchical representation of --

MS. ALLEN: You have no obligation to speculate on this, but answer the question.

A. They basically have identified the kinds of things I would have identified in the parenthetical after the two words "physical verification," as design rule checking, layout rule checking and logic versus schematic checking. So those are the kinds of things that are associated with physical verification.

Q. So those are -- Well, what is design rule checking?

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A. After you've made a physical layout, there are design rules that you specify for a given process as certain things that you can and cannot do. There are geometries that might be separated by a certain amount, line widths that must be a certain size, reservations for particular structures like vias. And the design rule check is a tool that searches through the representation of the physical layout to see that all of those rules are satisfied. It tells you if you have any places where you have made a physical design that would be a problem when you try to build this thing, given the process, or not.

Q. Okay. What is logical rule checking?

MS. ALLEN: I have the same series of objections.

A. I interpreted the "LRC" as "layout rule checking," and I would have said it's very similar. I guess there may be -- you may be correct. Again, I'm not sure what whoever it was that did this thing meant by that. But I took that to be layout rule checking, and that's what I would have considered it to be.

MS. ALLEN: Again, you have no obligation to speculate.

THE WITNESS: I understand.

A. It would be similar to design rule checking as in the physical layout for the device.

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Q. What about -- layout versus schematic was what you understood "LVS" to be?

A. I think so.

Q. Okay.

A. My understanding of that was that that was an attempt to extract from the layout a circuit, sometimes called circuit extraction, and compare that circuit against what a schematic representation of the circuitry should have been to ensure that when implemented in physical form that this device will have the appropriate circuitry.

Q. Have you heard the phrase "geometry manipulation" before?

A. I don't --

MS. ALLEN: Objection. It's outside the scope of the Declaration.

A. I don't recall that particular phrase, no.

Q. Okay. Have you heard -- have you ever heard of any of these acronyms that are shown under "Geometry Manipulation," as "RET," "OPC," "PSM" and "SB" used in connection with ASIC design?

MS. ALLEN: Objection. It's outside the scope.

A. No.

Q. Have you heard the phrase "analysis" -- or the term "analysis - slash - extraction" used in connection with chip design or any of those others under "Analysis/Extraction" used

in connection with ASIC processing?
A. I've heard those terms.
MS. ALLEN: Same objection.
Q. What does "analysis" mean?
A. Well, it can mean a hundred-thousand things. It's some form of analyzing the device at some stage of representation.
Q. And why would you analyze the device in the ASIC design process?
A. Again, many different reasons.
MS. ALLEN: And you have no obligation to speculate as to this exhibit.
Q. What does extraction mean in the context of ASIC design?
MS. ALLEN: Same objection. It's outside the scope, and you have no obligation to speculate.
A. Extraction -- and I gave you an example of a form of extraction, and I used it in circuit extraction.
Generally, I associate it with taking a given representation and sort of backtracking to see if it compares with a higher-level representation of the product so that you can be sure that when you move from one representation to the next that you did it in a way that maintained the design integrity.
Q. So is it like layout versus schematic kind of in

that regard?
A. I --
MS. ALLEN: I'm sorry. Can you repeat the question.
MR. KELLEY: Is it like layout versus schematic in that regard I believe was the question.
MS. ALLEN: Same objection. It's outside the scope. You're not obligated to speculate as to this exhibit.
A. I characterized to you earlier that I view layout versus schematic comparable. If that's what the consortium meant by it, I -- you know, it's a form of extraction.
Q. Are there other forms of extraction that you're familiar with?
A. There --
MS. ALLEN: Objection; outside the scope of the Declaration.
A. There are other steps that people have used in my experience that I might call extraction. I'm not sure whether they would or not.
Q. Okay. And what were -- what are these kind of steps we're talking about?
A. Any type of verification, as I just explained to you, where you take a representation at a lower level and backtrack to see if that representation still comports properly with the preceding representation.

Q. Okay. So am I correct that that kind of verification can be done only when I'm -- when I've actually got my physical geometries defined?
A. No.
Q. Okay. So when else can it be done?
A. Well, again, whoever did this, if you go back up to the third step from the left, they talk about formal verification. In a sense, that's a form of extraction. It's comparing two representations to make sure that they -- that they properly agree.
You can do verification without doing extraction; but one way to do verification is to do extraction and compare, as I say, two different representations at different levels of the process to see if they agree.
Q. Okay. In formal verification, what are the two different -- what are the two different representations that are being compared?
MS. ALLEN: Same objection.
Could I just do a standing objection so I don't keep -- I'm happy to do that.
MR. KELLEY: If you want to object -- if you want to object and you really think this is outside the scope, keep objecting. I think your objection is frivolous, but that's okay.
MS. ALLEN: Well, my objection stands. It's

outside the scope of the Declaration. You have no obligation to speculate as to this exhibit.
A. Well, they've placed "Formal Verification" here at the logic stage; and when you say "formal verification," that's generally a mathematical process where somebody goes in and looks at the forms of the representation.
Generally, that two-word term is used at a higher level where you are dealing with more abstract representations at a -- a block level or a transfer level or maybe even in a functional description and you're trying to see that when you move from a functional description to a transfer level description are those two really the same over some universe of input and output characteristics. So that's what I would think it would mean relative to the term "formal verification."
Q. Okay. Have you heard the phrase "design planning" used in connection with the ASIC process -- in the process of ASIC design?
MS. ALLEN: Objection; outside the scope. There's no need to speculate what this exhibit is.
Q. Set aside the exhibit. Have you heard the phrase?
A. I don't think I've ever heard that called out as a step.
Q. The question was slightly different. Have you ever heard that phrase? So you haven't heard it called out as a

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separate step. Have you ever -- have you ever heard anyone use that phrase to refer to something during the process of ASIC design?

A. I'm sure in my experience somebody said, "Well, I'm planning my design" at some point. But I don't -- again, I don't -- I don't assign any specific meaning to that two-word term in the sense that I do some of the other terms --

Q. Okay.

A. -- that show up in this exhibit.

Q. You're not -- are you familiar with CAD tools that are identified in -- a family of CAD tools that would be identified as design planning tools?

A. Well, I'm familiar with some of the tools that are listed below this. Again, that's why I asked you about a time frame. Some of these tools seem pretty recent, at least in my experience. So I'm assuming that this thing is actually fairly recent in its hierarchy and not necessarily relevant back to the view of the EDA industry in the mid '80s and early '90s. But I'm familiar with those types of tools that are shown below it on this exhibit.

Q. Which tools are you familiar with?

A. I think I've actually heard of the tool Chip Architect. It talks about floor planning. Certainly, people did floor planning as part of the movement from representation to representation. The other tools that are listed there I'm

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not familiar with. They look like brand names that somebody produces.

But I understand that -- what I gather whoever wrote this intended to represent by this block labeled "Design Planning." I probably would have, in my view, moved it further down in the process --

Q. Okay.

A. -- but it's okay. I mean, certainly people do that, and I did that. I just don't know that I ever thought of it as being a particular step in the process.

Q. You don't think that, what, floor planning is a particular step, or you don't think of the words "design planning" as a particular step?

A. I just think I did a floor plan as part of the physical process. Okay. So I would have tended to lump that in with probably a -- if I had to do it, some form of physical representation, or I might have actually done the floor planning at the very beginning to try to understand the size of the die that I wanted to use. It's hard to do that until you have an understanding for what the actual process that you want to use is.

Q. Are you familiar with the phrase "emulation" in connection with ASIC design?

A. Yes.

MS. ALLEN: Objection; outside the scope of the

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Declaration. You don't need to speculate.

Q. What is it?

A. It's used at many different levels. But it's an attempt to get a computer to model the behavior of some representation of the product.

Q. Is emulation an essential part of ASIC design? Can you do without it?

MS. ALLEN: Objection; vague.

A. I don't know of any valid approach that would not make use of emulation.

Q. We were discussing physical verification. I mean, is that an essential part of ASIC design or --

A. I'm sorry. Your voice is low.

Q. I apologize.

A. I couldn't hear you.

Q. We discussed physical verification under which we talked about DRC, LRC and LVS. Is that an essential part of ASIC design?

A. Again, I guess you could imagine a design process that didn't do it, but I think it would be an invalid process. I think it -- it is an essential step.

Q. Am I correct that it's essential because if you didn't do those things, you wouldn't have any ability to predict whether you had a good design that would actually operate?

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A. That's, you know --

MS. ALLEN: Objection. It's outside the scope of the Declaration.

A. Again, you'd be flying blind. You would just be assuming that something was okay without checking to make sure it was as okay as it could be by using such verifications.

Q. We also talked about formal verification. Would you regard that as an essential step in the ASIC design process?

MS. ALLEN: Same objection; outside the scope.

A. At least during the period that I was working - and by that I mean the '83 to, say, '95 time frame - formal verification was only beginning to be available. So clearly there were lots and lots of ASICs that were done without any formal verification tools available.

Now that some reasonably solid formal verification tools and techniques are around, I can't think of any reason to avoid using them. If I were managing a design process today, I probably would consider them to be very important.

That's a long way of saying I don't know whether to say that's essential or not; but it certainly -- those tools, since they're available, I would recommend to anybody who is considering doing an ASIC that they be utilized.

Q. So it's good judgment to use them; but if you didn't

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use them, you might get it not operating at the other end of the process?

MS. ALLEN: Object; compound and to the extent it mischaracterizes prior testimony.

A. What I said to you is that I know of lots and lots of ASICs that were designed by myself and others absent the use of formal verification because it wasn't -- it wasn't commonly available. It was still kind of an abstract, university, academic concept at various points in my career. But now that it's here, it's certainly very useful in assuring that the goal of trying to make the silicon that you make will actually work the way you want it to from the beginning.

Q. Okay. Am I -- I'm not asking you to adopt this drawing. But to the extent that they show "Physical Verification" as a step that followed after "Logic Design/Synthesis," is that typically -- would it make any sense to do physical verification before logic design synthesis?

A. I don't think it would.

Q. The same question about floor planning let's say?

A. I think I said earlier that you might actually have in mind a die size, for economic and technical reasons, almost from the beginning of the process. So you could do floor planning, at least done at a high level, in the early stage to sort of size the overall goal.

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Q. But after synthesis, you would return to the floor plan and make further revisions or do more floor planning at a more detailed level?

A. Well, I think I would tend to think of floor planning as a continuously evolving process as you get further down the sequence of representations that I just referred to you earlier. As you become more bound to specific technologies and strengths, that might force you to modify the floor plan or to realize it in some other way to become more clear. So I would say that that is an evolutionary process.

Q. Okay. So am I correct in understanding that floor planning is something that you probably return to at multiple points during the ASIC design process?

A. You can argue that the place in route is a form of floor planning. So, yeah, I think that's something under consideration throughout the process until you get maybe almost to the end.

Q. So some of those that consist of floor planning are likely to occur after logic synthesis?

MS. ALLEN: I missed the question.

Q. Some of the places where you do floor planning are likely to occur after logic synthesis?

A. I think, again, you may not even address it until after the logic synthesis and --

Q. What about --

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A. Let me finish my answer.

Q. I'm sorry.

A. Or you may elect to have addressed it earlier but be forced into doing some sort of modification of the original contracted form.

Q. Okay. What about simulation? Where does that fit into this process?

A. You can simulate --

MS. ALLEN: It's the same objection. It's outside the scope. And you don't need to speculate as to this exhibit.

A. I'm not addressing relative to the exhibit.

Q. I'm not asking you to.

A. I took that question to be just based on my knowledge of the art.

You can simulate at almost every level.

Q. Is it correct that it is probably -- that you're going to simulate after -- after logic synthesis? Although you may simulate before that, no design engineer is going to not keep simulating after logic synthesis?

MS. ALLEN: Objection. It calls for speculation. It's compound and vague.

A. They may use some -- some form of simulation at a later stage.

Q. Are you familiar with any designs of ASICs where

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simulation wasn't used after -- after logic synthesis?

A. Well, the reason I'm -- I said "some form" is, you know, when you think of the higher levels, you probably are simulating the entirety of the device. As you get further down into the physical binding, it may be prohibitive to simulate the entirely of the device at a low level or an integrated circuit level or even a physical level. So you may simulate key pieces of the device or you may abstract in and maybe do a timing analysis that's -- a critical path type of analysis that, in a sense, is a form of simulation to estimate critical path delays and things of that nature.

Q. You say "in a sense." I mean, you assume the sense that I'm only simulating part of the circuit, right, as opposed to the whole chip?

A. Yes. I mean, there may be people who have competence and resources such that they can do a detailed physical simulation of a modern, multi-million transistor chip. At the time that I was working in the field, that would not have been practical. So you would have used, say, an integrated circuit simulator like SPICE only on portions of the device where you felt it was important to model at that level to get an understanding of the physical character of the product, but maybe you used a higher level of simulator that worked off of a hardware description language like Verilog or the HDL to simulate functionally at the top level.

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Q. Am I correct that one of the important things about -- or one of the important approaches of simulation is to determine the timing of signals and whether this is going to operate with -- with real circuit timing, signal timings, as the design gets increasingly more specific about the technology used?

MS. ALLEN: Objection; compound. This is outside the scope of the Declaration.

A. I probably wouldn't necessarily agree with that statement. That's different from disagreeing with it. But there's a lot of simulation that has little or nothing to do with detailed timing analysis but addresses more functionality, and there are ways to do timing assessments without doing what might conventionally be called simulation.

Q. All right. So I understand it, one of the purposes of simulation is a functional -- a functional testing of the circuit. Is another element of simulation doing a timing -- timing analysis?

MS. ALLEN: Same objections.

A. I don't disagree with that. I'm not buying into that statement in that there are ways to do timing assessment that might not be thought of as being simulation per se.

Q. Okay. And what are those things?

A. Critical path analysis that are more modeling in a sense where you make estimates of what kind of delays along

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the path there are going to be.

Q. Where would that critical path assessment take place? I mean, is that going to be something that's going to come before synthesis or after synthesis?

A. It's probably -- Again, you're trying to separate a fairly amorphus set of processes into you go to Step A and then Step B and then Step C, and it's almost like you'll never revisit Step B, at least the way I'm interpreting your question.

I think you can do some estimates of timing at a fairly early stage; but then as you get to the point where your design is more bound to the physical characteristics of the technology in which it's going to be implemented, you do better estimates of timing and based on those, you may have to go back up to a much higher stage and redesign. So that's why I'm saying I don't -- I don't think it's -- it's not as cut and dried as you seem to be --

Q. So --

A. -- implying in your question.

Q. So I might do some timing analysis before synthesis, but it's also the case that I'm likely to do some timing analysis after synthesis. Is that correct?

A. I think that's possible and maybe even likely.

Q. Would it be good design practice not to do any kind of timing analysis after logic synthesis?

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A. I wouldn't think so.

Q. Are you familiar with the phrase "GDS-II"? It's actually not on -- I don't believe it's on that.

MS. ALLEN: Objection. It's outside the scope of the Declaration.

A. Is there a question?

Q. Yeah. Are you familiar with the phrase "GDS-II"?

A. I think so.

Q. What is GDS-II?

A. It's been a while since I've worked with that term, but it seems to me that dates back to an early physical design system produced by a company called Calma. That's C-a-l-m-a. And they came out with a language -- I used to remember what GDS -- it was like "geometric design specification" or something like that, and then they came out with GDS-II. But it was a geometric or physical layout state of representation standard, and I think it may still be in use. I think there are a couple of others that may have supplanted it. But that's my recollection as to what the GDS-II is.

Q. So it's a format that would be used in transferring data that -- or transferring design data that's described in terms of geometries?

A. That's my recollection. My recollection is that it came out of what I previously referred to as the polygon-pushing school of design. So it was one of several

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ways of representing the detailed geometric data for the physical design.

Q. Are you familiar with the acronym MEBES?

A. Oh, gosh.

MS. ALLEN: Same objection; outside the scope of the Declaration. You don't need to guess or speculate, either.

A. I have some recollection of that, Mr. Kelley, but I don't -- as Ms. Allen has cautioned me, I would be speculating to tell you what I think. I mean, I have something in mind, but I haven't -- I haven't seen that term in quite a while, but it's -- I think it's -- it's a term of the more physical end of the art.

Q. Okay. Let me get you to go back to Exhibit 1, your Declaration.

A. Okay.

MS. ALLEN: What did you say?

MR. KELLEY: I was muttering to myself because I wasn't -- I couldn't find it, but I found it.

MS. ALLEN: Okay.

Q. Page -- Well, there's no page number. It's Page 4, the one that's got the Paragraph 10. I'm interested and I wanted to talk to you about lines -- well, everything in Paragraph 10. But Line 10 to 13 reads as follows: "From my own design work, and my experience and knowledge of the work

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of others in the field, I believe the following process steps are an essential part of the manufacture of ASIC products." And then you go on and you identify "A" through "G" as process steps.

Am I correct that this is not a complete list of essential process steps in the manufacture of ASIC products?

A. Well, I take your question to mean are there other steps that would be considered essential?

Q. Yeah, that's correct.

A. I mean, I'll kind of give you the same kind of answer President Bush gave last night. When he was asked "Have you made any mistakes," he said, "I'm sure I have, but I don't know what they would be."

I think the better way for me to answer that would be is if you wanted to propose another step that you have and in some cases would I consider those to be essential or not.

I think this is a reasonably good parsing of the sequence of the steps that people use, but I don't know that I've attempted to identify every other step that someone might use at some stage or even characterize it as a separate step. So I don't know how to answer your question.

Q. Okay. Well, let me just go to Step G, which reads, "Using the mask data to create the set of multiple masks

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required for producing the circuit layout on the silicon die to form the ASIC product."

A. Okay.

Q. I take in that step you're talking about creating masks. Right?

A. Yes.

Q. You don't mention -- You don't then go into the various steps involved at the foundry to create the ASIC. Is that correct?

A. That's true. So I haven't ended up with silicon. So I guess "H" would be -- and I stopped here, would be the actual fabrication of the silicon in the foundry --

Q. Okay.

A. -- or the fab. It doesn't have to be a foundry.

Q. Is there any reason you didn't go to "H"?

A. I'm sorry?

Q. Is there any reason you didn't include "H"?

A. Not particularly. I just stopped with mask data to make the masks.

Q. Masks are -- Well, can you briefly describe what masks are?

A. Well, again, I tried to allude to you earlier that the mask technology has become increasingly complex as physical sizes have gotten smaller and processes have become more complicated. But you -- you tend to use a series of

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lithographic steps. You tend to use light. There are other technologies. But you can think of it as photography.

The masks are a series of images which control the flow of light to a properly prepared surface on the silicon and, as a result, allow certain physical and chemical changes to take place in a sequence of steps, each mask controlling what's going to happen at a particular stage in the manufacturing process.

I can expand on that if you would like me to or you can ask me further questions.

Q. No. That's fine.

Masks are used multiple times, correct, in making multiple ASICs -- or making multiple copies of the same ASIC?

A. They can be.

Q. It would be --

A. I'm sorry?

Q. Never mind. Strike that.

They can be. I mean, isn't it -- isn't that what typically is done?

A. That's typically -- part of the reason that I gave you a "can be" is that there's step and repeat approaches in which they're used multiple times even in making a single wafer, and then there are full masks that are projected only once. There's been, again, an evolution of the technology

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over the years as to which of those techniques are used. But you would expect a set of masks to be capable of being used over the lifetime of the manufacture.

Q. Now, the mask itself isn't, you know, incorporated into the final ASIC that's delivered to the customer. Is that correct?

MS. ALLEN: Objection; vague.

A. I have no idea what you just said.

Q. Yeah. The mask -- the physical mask itself is not incorporated into the ASIC that actually is produced by this process, is it?

MS. ALLEN: It's still vague. The objection is it's outside the scope of the Declaration.

A. Do you mean do they deliver the mask?

Q. Uh-huh.

A. Well, I guess it could be part of what the customer asked for when they got their products from a fab, that the masks were returned to them. Again, I -- I don't even --

Q. Well --

A. -- there must be a meaning to your question and I can't figure it out.

Q. Let me clarify. I'm sorry.

The ASIC, the semiconductor -- the semiconductor device, the ASIC, doesn't actually include -- the package doesn't incorporate part of the mask, does it?

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MS. ALLEN: Objection. It's vague.
A. Well, I mean, in a sense it's represented in the masks because those are used. But the physical masks themselves would be kept at the foundry, if that's what you're talking about.
Q. So the mask is a representation of the design that's formed in the ASIC. Is that correct?
A. Yes.
Q. Okay. But the mask itself physically is something separate from the ASIC. Is that correct?
A. Well, that's -- I think that's true. That's like saying that - I don't know - like a negative is not exactly the same thing as the print that's made from the negative and delivered to somebody who wanted to see the picture. Again, I find that question to be so nonsensical I have trouble understanding it.
Q. Well, actually, it's not nonsensical. I think it's just really simple. I agree it's kind of simple-minded.
All I'm trying to point out is that there are two physically different things. The mask has a physical or existence separate from the ASICs that are produced from it. Is that true or not?
A. Yes, that's true. They both represent the same thing. I mean, I tend to think of the masks, as I mentioned earlier, as a hierarchy -- a hierarchy of the representation.

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They are a representation, but they are physically separate from the die itself that -- that is the representation of the ASIC itself.
Q. There are some multiple masks that are used in forming an ASIC. Right? There's not just one mask. Is that correct?
A. Typically, there's a set of masks.
Q. And each mask corresponds to a different layer or part of the fab process. Isn't that correct?
MS. ALLEN: Again, objection. It's outside the scope of the Declaration.
A. Yeah. These days it's really kind of hard to talk about layers because there are a whole lot of processes that -- it's not as simple as it used to be back in the '70s and the early '80s. But each mask represents a point in the overall manufacturing process maybe is a better way to put it.
Q. So -- so each mask contains some information about the design, but it's certainly not all of the information about how the design is going to work. Is that correct?
A. That's true. It's the totality of the mask set that represents the design in that form of representation.
Q. Let me skip back up to Step A, which is "Describing a series of functions that are to be performed by the desired ASIC product to be manufactured."
How would somebody building an ASIC do this

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describing? I mean, what does that physically correspond to? What acts does that correspond to?
A. Over the years, there have been a variety of ways to do that. Today a very common one would be a higher -- a hardware description language like Verilog or the HDL. But there are flowcharts, and there are timing diagrams. There -- It could be a schematic diagram at some high level, a transfer level diagram.
Q. How about a design spec?
A. I tend to think of -- Well, it could be if it was tightly enough written. It could be if it were functional or structural in its characteristics enough that it gave a clear binding as to what the result would be.
Q. So you said the metric for determining whether -- these words here are describing a series of functions. Is it its completeness and its detail, or what -- how are you -- how are you identifying what's -- what is describing a series of functions and what is not quite?
MS. ALLEN: Objection. That's vague, and I think it's misstating his prior testimony.
A. You asked me about a design spec. I didn't have a design spec in mind when I wrote Step A. I tended to think in terms of the types of descriptive tools that I had experience with or that I was aware of people using today. And I had in mind, for example, and probably the best example I can give

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you, is hardware description language that you would define what the device is supposed to look like functionally. I know you're aware from my prior experience with you personally, you can do that description either functionally or structurally or in some combination of both. That's what I had in mind, that stage of the process.
Q. Okay. So -- so you weren't intending with "A" to capture timing diagrams or -- or engineering specs?
A. No, I wasn't trying to exclude those. I was just giving you a good example of what a design spec is. I think flowcharts are an excellent way or state diagrams or tables. There have been a variety of tools that designers have had available over the years in order to do the initial description of that.
Q. So those are all possible in describing the series of functions. And when you said -- you say in your Declaration that the step is essential, are you saying that it's essential that one write HDL, or are you saying that it's essential that one provide some kind of description, whether you do that using HDL or flowcharts or a similar state table that you mentioned that you -- which of those two is it?
MS. ALLEN: Objection; compound and vague.
A. Yeah. You know, you've given me a universe of two things to answer the question. Within the scope of that universe, it would be the second answer. I did not intend to

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restrict it to HDL usage.
Q. So HDL usage itself isn't necessarily essential, but it is essential that one describe a series of functions in some manner?
A. In some manner that's sufficiently clear and complete to allow Step B to take place.
Q. Okay. Step B is "Performing logic synthesis to identify the logic blocks needed to achieve the desired functionality."
Does this encompass what we've here referred to as the manual technology binding, or is "B" limited to computer -- computer-aided logic?
MS. ALLEN: It's compound. I object.
A. I think it's fair to say that I had in mind -- let's characterize it as a preferred embodiment when I thought through this sequence.
In the context of your question, however, I think people can, and did, and probably still do, logic synthesis in a manual fashion. But certainly my preferred embodiment concept, Mr. Kelley, was that they would do this with a computer-aided design tool, commonly called a logic synthesizer; but I don't think that that's necessarily the only way it could be done.
Q. So they can do it by hand or using a computer. Is that correct?

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A. Yeah, I think they could do this stage. They could essentially manually do the same thing that the logical synthesis computer-aided design tool will do. They could map from the functional description in Step A to the logic blocks that are needed to achieve that design functionality.
Q. Back when I was a working engineer, we used to come up with schematics and put AND gates and OR gates and so forth to create a circuit description.
I take it that if somebody wanted to build a circuit that way and not use logic synthesis that way, it would be manual logic synthesis within the meaning of that language that you've described in Step B. Is that correct?
A. Under the rubric that I've used in Step B, which is logic synthesis, and I've defined what I meant by that in the rest of Step B, that could be done with a computer-aided tool or it could be done manually.
Q. Okay.
A. But that's an essential part of the manufacturing process.
Q. What -- what is -- what is your understanding of the phrase "mask data"?
A. It's data that can be used to manufacture the mask. It would be the geometric characteristics of the mask.
Q. Okay. You indicated earlier that -- and we talked about whether something should be included and whether there

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should be steps that are above "A" in the process that might be included. Let me float a couple by you and get your reaction to whether you think they qualify as essential -- an essential part of the manufacture of ASIC products.
MS. ALLEN: I object that it's misstating prior testimony.
Q. Here's one. How about assessing customer interest in the possibilities of the product? Is that an essential part of the manufacture of the ASIC product?
A. I wouldn't think it was, but I think it's important. You probably wouldn't want to spend a lot of money building something for which there's no market. But I personally don't think that's essential.
Q. Okay. How about doing a product -- doing an initial -- you know, a high-level design of the product --
MS. ALLEN: Objection --
Q. -- an initial engineering statement of what the product is going to be?
MS. ALLEN: Objection; ambiguous.
A. You've changed horses in the midstream of the question. Why don't you try that again.
Q. Yeah. How about doing a high-level specification to start with to determine what the functionality of the product is going to be?
A. Again, I think I've been involved in products where,

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when we started, we may not have even had a clear idea of what we were trying to do. I don't know that that's essential. It's certainly important to do that. As a manager, I would expect that to be done. But I don't think of that as being an essential part of the manufacturing process.
Q. What about purchasing the tools for the designers and the equipment -- the CAD equipment the designers are going to use? Is that an essential part of the manufacturing process?
A. I wouldn't consider that -- Again, it's something that one assumes as a given, that there's a floor and some computer facilities and desks and things. I don't consider that as part of the manufacturing process for the ASIC design itself.
Q. It's -- But is it essential that those things have happened?
A. I mean, you're going to have to clarify.
MS. ALLEN: Objection. I don't understand.
A. Yeah. You don't have to purchase them. You can lease them or borrow them. If you've got -- if you're going to do -- if you're going to use a tool to do a step, you've got to have access to the tool.
Q. So is it essential to have somehow arranged for access to the tool?
A. That question is --

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MS. ALLEN: Objection. I think the question is sort of ambiguous and almost calling for unfair inferences. I don't want to give speaking objections. I'll just leave it at that.

A. I would not consider it to be an essential part of the manufacturing process, but I would consider it essential that you have in place the resources necessary to start the process.

Q. Okay. So arranging for the tools is -- it's essential, but it's not part of the manufacturing process. Is that correct?

A. I would assume that the individuals that are necessary to do it would be in place and that the skill sets would be there. Those are not things that I listed in my set of essential parts of the manufacture of an ASIC product.

Q. That's what I'm trying to get at. Am I correct that the reason that you didn't list them is because it's not part of the manufacturing process?

A. I don't -- I mean, the document is my opinion, and that's what my opinion is. You're asking me is it essential that the earth exists and that we have oxygen and electricity and -- I mean, those are all things that have to be in place before you start the manufacturing process. So are they essential? In a sense, they are, but I don't consider them to be an essential part of the process. It's a

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precursor.

Again, I don't even -- that question is so nonsensical to me that I have trouble even understanding how to answer it.

Q. Well, what I'm trying to get at is a distinction between an essential part of the process and -- or essential to the -- to the process -- essential precursor to the process and whether they're an essential part of a manufacturing process. And I take it that you are saying those things are necessary, yes, but they're not part of the manufacturing process?

A. That's a reasonable understanding of what my opinion is, yes. There are -- there are things that you have to have in place in order to accomplish the steps that are the essential parts of the process, but I don't think of those as being part of the process of manufacturing an ASIC product. I just assume those as a given at the start of the process.

Q. Are you familiar with the phrase "ASIC design"?

MS. ALLEN: Excuse me?

MR. KELLEY: ASIC design.

A. I think so.

Q. Is that distinguished, in your understanding, in any way from ASIC manufacture?

A. I think in the context of my Declaration that I've included the two together as being the totality of the

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manufacture of the product.

Q. You included the two together. So you've used them as synonyms?

A. I think if you were to break out the steps that are here that some of the earlier ones would be a design-oriented step in the overall manufacturing process. But I've kind of combined them into my understanding of what I've referred to in Paragraph 10 as the manufacture of ASIC products.

Q. Have you heard people draw a distinction between design and manufacture?

A. I think I have.

Q. And here you didn't draw that distinction; you put the two together, that something was design and it was also manufacture. Is that correct?

A. Yes. I considered that if one sets out to manufacture an ASIC product that one has to do the design steps at the early stage of the overall manufacturing process in order to be able to reach the end of the process and actually physically make the device. So I characterized the entirety of those steps as the process of manufacturing the ASIC product. That's a reasonable characterization.

Q. Is there any reason you didn't distinguish between design and manufacturing?

A. I was asked to deal with the overall totality of the manufacture of an ASIC. I consider those, both the design

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stages in that process and the final foundry-type stages, to all be essential parts of the manufacture of the products. The way the question was asked of me I felt it was appropriate to combine those into the steps that are shown in the Declaration.

Q. Okay. If it was important to the issue for the Court to distinguish between design and manufacture, would -- would you -- would your Declaration shed any light on where that line should be drawn?

MS. ALLEN: Objection --

A. I have -- Go ahead.

MS. ALLEN: Objection. That question is vague and ambiguous, and it somewhat calls for speculation as to what's going to be important. Go ahead.

A. I have to understand whatever question the Court was trying to address in a better terminology than the way you phrased it. I don't understand what importance there was associated with it.

Q. Let me ask it this way: There's nothing in the Declaration, as written, that addresses that distinction. Is that correct?

A. I think that's incorrect.

Q. Okay. Tell me what -- what part of the Declaration addresses the distinction between design and manufacture.

A. Paragraph -- Well, you've stated in your question an

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assumption that the Declaration rebuts, which is that it's appropriate to separate the manufacture of an ASIC into a design phase that's completely separate from a manufacturing phase. So, as I said in Paragraph 10, I think that when one considers the totality of the manufacturing process, while it has stages that are design oriented, the beginning -- really, they play into the overall manufacturing process. So I don't see a separation here.

Q. Okay. But what I'm -- what I'm asking you is if you're wrong about that and it is important to distinguish between design and manufacture, is there anything in your Declaration that would help draw that distinction?

A. Well, I don't think I'm wrong about that, and so I don't -- I don't know how to address that. The Court should consider the Declaration within its four corners for what I've said here, and I would be happy to answer -- answer any questions that the Court may have to clarify it. I think my opinion is here. If the Court elects to reject that opinion, that's their decision. I don't know how to speculate as to what would happen there. I don't have an answer for you.

Q. Okay. Do you have -- you mentioned -- I'll have to paraphrase. You mentioned there were some things, I think, earlier in the process that were more design oriented, I think you said. Is that correct?

A. You asked me earlier had I heard of a distinction

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being made between design and manufacture. I think if one looked at the earlier stages here where I've talked about describing a series of functions, et cetera, that those are stages that people would say are being done by designers. Although, certainly mask design is a stated design art. Those would be stages that would -- would be more design oriented in the overall manufacturing process. That's about the best I can --

Q. Well --

A. -- answer your question.

Q. When you say "those stages," which stages are you referring to?

A. Oh, probably -- Well, it's hard to say. I mean, you can apply the rubric "design" to every one of these stages, every one. You can do functional design, logical design, circuit design. There's an aspect of design to form the netlist. There's an aspect of layout design. You can do mask design. So really I guess maybe I need to clarify what I've said earlier. I think any of these stages could be characterized as design within the overall manufacturing process.

Q. How about "G"? Does it make sense to talk about "G" as design?

A. Yeah. I think there are people who would say that even once you have the mask data that there would be some

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design steps. I think mask manufacture has become somewhat of a black art in modern technology. I haven't -- I'd have to go back and try to look and see, in the relevant time frame, how -- how automatic the ability to use mask data to create the masks themselves was back in that time frame. I'm not prepared to give you a detailed answer on how automatic that step would be in the appropriate time frame.

Q. I'm not -- I guess the process flows are going to be different over the time frame from '80 to the current. Is that correct?

A. Yes.

Q. Okay.

A. And in any one of these steps, I think things may have changed a bit. I mean, certainly the nature of the masks has changed as the process technology as changed dramatically.

Q. Do you think what people would characterize as design oriented has changed over that point in time?

A. No, I don't have an opinion about that. As I said, I think, really, when you look at each one of these steps, they all involve design within the step itself.

Q. We had added -- I think sort of informally we had added an "H," which was manufacture of the ASIC itself at the fab. Is --

A. Yeah.

Q. -- that correct?

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A. That's correct.

Q. Is that design oriented?

A. Well, it's been my experience that at the fab stage, people find out that there are problems with the device, either in its manufacture or functional performance or timing, and, as a result, a design revision may be forced upon that. So, in a sense, there are some aspects that relate to design.

Q. There's some aspects that relate to design. But would you -- would you characterize the fab process as being design oriented?

A. There are people who do nothing in their lives except design the layout of fabs. But relative to the design of the ASIC process itself, I probably wouldn't think of that as being part of what I would tend to characterize as design. But that may be, in part, because of my own view of the art.

I've -- While I've spent time in fabs and all, that's something I -- I probably have not contributed to personally as a designer. So I would have to take my answer from my own point of view. Other people might actually consider that to be part of the design process.

Q. Have you ever --

A. There are issues like design centering which attempt to make sure that, over the range of parameters of the manufacturing process, the design will still operate. So I think there are design aspects there. It's just that I

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personally am not as familiar with it as I am the overall process.

Q. Have you -- have people that you work with and encounter, have they -- have those folks ever referred to some ASIC fab and a foundry as -- as design that you can recall?

MS. ALLEN: Just can you repeat the question. I'm sorry.

MR. KELLEY: Sure.

Q. Professional folks, the people that you've encountered in your professional career, have -- are you familiar with any instance in which those folks, or anyone that you've encountered, has referred to semiconductor manufacturing at the fab as being part of a design process?

A. Well, I mentioned to you this characteristic called design centering where you interact with the fab people to try to understand what the range of parameters in their process is and how tightly they're controlled and how they think things are going to happen during the process. And I certainly have -- am aware -- it's not something I personally have done a lot, but people interact with the fabrication engineers at the foundries and fabs and may, in fact, go back and modify their design of the physical characteristics of the ASIC, if not even the functional or logical characteristics, to try to get better yields and better performance over the range of process parameters. That's a long way of saying I think so to your question.

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Q. Okay. Design, other than in the context of design centering, have you heard people refer to the process of making a semiconductor as -- as semiconductor design, in your --

A. I don't --

Q. -- experience?

A. I don't think so.

Q. Okay.

A. I don't have any prior -- any other recollection of that other than that aspect of it.

Q. Okay. Design centering is something that happens before the ASIC is actually fabricated, isn't it? Is that correct?

A. I think it can happen before or during. I mean, as you run processes and you begin to understand, you can yield data and other types of information, and you can use -- use what you're finding to go back and try to recenter the process if you find out that's it's not working. And I think -- again, I think of all of these steps can interact, at least in the sense that at any stage, you may be forced to go back to a previous stage and do some modification.

Q. Maybe I didn't understand what design centering is. Is design centering actually changing my circuit design?

A. Not necessarily a circuit design. You might. But you may change your physical layout --

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Q. Okay.

A. -- to try to achieve, over a broader range of process areas, acceptable functionality and timing.

Q. So I am going to change my mask. Is that correct?

A. It could. Yes, it could -- it could affect the characteristics of the mask. That, to some degree, is why I was telling you earlier that while I know something about the details of Step G, that's an area that I personally don't have as much experience with as I do others. And it may be that there are other adjustments that experienced mask design engineers can make for the same set of mask data that they can actually produce different sets of physical masks based on their knowledge of how they can improve the -- the yield when those masks are used to make this ASIC product.

Q. So design centering would be -- and you had mentioned earlier that there were design elements to Step G, which is making the mask. I take it that design centering might be one of those -- one of those elements. Is that what you're suggesting?

MS. ALLEN: Objection. That misstates his prior testimony.

A. I would -- I think that in this legal context, I shouldn't speculate about something about which I only know a little bit. It -- the answer -- best answer I can give to you is it might be, and that's not a very useful answer. So that's the answer that you can accept. It might be. I'm not a mask design engineer personally. So it could.

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Q. You don't know one way or the other whether design --

MS. ALLEN: Objection; asked and answered. I'm sorry. I'll let you finish.

Q. You don't know, one way or the other, whether design centering is going to impact the process of -- that's described in Step G or not. Is that correct?

A. I don't know with --

MS. ALLEN: I will keep my objection; asked and answered.

A. I don't know with assurance. I think it might. That's the best answer I can give you. I can't exclude it. But I think somebody who is a mask design engineer would be a better person to ask about that. And I think that issue will change dramatically over this period of time that we're talking about.

Q. Design centering isn't something that's going to affect Step H, the actual fab of the ASIC? I mean, you were using information that we know about how these processes work, but I don't actually change the process as a result of design centering. Is that right?

MS. ALLEN: Objection as to -- I think you

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might be misstating his testimony.
MR. KELLEY: Well, that's why I'm asking yes or no. I want to make sure I got it right or not.
MS. ALLEN: And I think the question is a little vague and ambiguous.
A. Well, I don't know if I would characterize changing the process as a direct result of something. I wouldn't call it personally design centering. But I do know that the process may be tuned up - I've had experience with that - to try to increase yields primarily from a timing point of view. So I think that -- that there are aspects of the manufacturing process, even at this mythical Step H, that can be adjusted to try to achieve the best possible product at the end of the manufacturing process.
Q. Have you ever heard anyone refer to that kind of fine tuning as design centering?
A. I don't think I've heard it referred to as design centering. I mean, maybe they do. I don't know. I -- That's not what I would refer to as design centering. But it certainly is an aspect of the overall manufacturing process.
Q. Have you ever heard anyone refer to that kind of tuning as ASIC design?
A. I think -- The answer I can give you is I think they would be comfortable with including it as a -- a portion of the overall manufacturing process for the ASIC.

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Q. Do you mean just folks who are at the foundries generally would be comfortable with that?
A. As part of the manufacturing process. Whether they would call that part of the design process or not, I think that would be -- it depends on how you explain to them the nature of the question.
Q. Okay. But you've never heard anybody at the fab refer to that kind of tuning as design centering?
A. I can't say that I have. I can't say that I haven't. Okay. As I said, I would agree that it's part of the overall manufacturing process. Whether I remember ever hearing anybody say, "Oh, that's part of the design," I don't recall.
MR. KELLEY: Do you want to take a little break?
THE WITNESS: Sure.
(RECESS TAKEN)
Q. (Mr. Kelley continuing) I want to talk about 10(B), this performing logic synthesis step. You identified it as an essential part of the manufacturing?
A. Yes.
Q. Am I correct that it's essential that you do logic synthesis, but it might be computer logic synthesis or it might be hand synthesis, what we called manual synthesis, I guess? Is that correct?

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A. I certainly had in mind, as I characterized it earlier, Mr. Kelley, as a preferred embodiment, something like a logic synthesis tool, because I'm familiar with those tools. But I think it could be done manually, as well, as I said earlier.
Q. And in Paragraph 9, you said that you have looked at the '432 patent?
A. Yes.
Q. And you believe that it describes and claims an integral portion of the manufacturing process utilized in the semiconductor industry for the manufacture of application specific integrated circuit - ASIC - products.
Do you have any view today as to whether the scope of the claims of the '432 patent extend to manual synthesis that we've certainly talked about?
A. I don't have any opinion about that at all. I haven't studied the claims to the point that wherein I would be able to form an opinion and give you an answer to that.
Q. Okay. So it might be or it might not be, as far as you know today?
A. I have no opinion either way.
Q. Okay. So then I take it you also don't have an opinion as to whether the '432 patent describes and claims an essential part of the manufacturing of the ASIC products -- Let me strike the question.

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I'll formulate it this way: You don't know whether in order -- as an essential part of the manufacture of ASIC products, one has to do what is described in the '432 patent?
A. I don't have any --
MS. ALLEN: Could you repeat the question.
MR. KELLEY: Can you read it back.
(Requested portion was read)
MS. ALLEN: Objection. It's vague and compound. You can answer it.
A. I thought I understood, but let me -- since you've raised the objection as vague, let me think through it. Let me play -- If you don't mind, I'll play your question back and see if this is right.
Q. Anything you like.
A. Okay. What I think you're asking me is given that I've given you a set, in Paragraph 10, of essential steps, do I consider -- whatever may be claimed as inventive in the '432 patent, do I consider that that's an essential -- that that process is essential to making any ASIC?
Q. Uh-huh.
A. I don't have an opinion on that today. I haven't studied the claims to that degree.
Q. Have you -- In your professional career, have you ever heard anyone discuss the distinction between design and

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manufacture?
A. I think probably so, yeah.
Q. And in those discussions, did people -- whether they did this formally or informally, did they identify some -- some method by which you would identify it and say that's the one for manufacturing and that's the one for design?
A. No.
Q. Okay. So what, sitting here today, do you remember about those conversations about the distinction between design and manufacturing?
A. I think there are people who do design with no goal to ever have it manufactured, you know, like teaching or something like that, that they just -- that they maybe stopped with Steps A -- maybe even Step A and that's all they do and they would say that they were doing ASIC design.
Q. Okay. Any other context for the words "design" and "manufacture" that you remember?
A. No.
Q. Do you remember any occasion on which someone writing a -- Well, strike the question.
Let me ask it this way: Do you remember any occasion on which someone doing what would be encompassed within Step A in Paragraph 10 said that they were performing -- told you that they were performing a manufacturing step or used manufacturing to describe something

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that falls within the scope of Step A?
A. I think it would depend upon the nature of the conversation, and I probably have had instances that would go both ways.
Q. Okay. Let's talk about instances where, in fact, you do recall that they used the word "manufacture" or "manufacturing" to describe the activities in Step 10(A).
A. I think if somebody had been asked as much as I was asked to define the totality of the process of manufacturing the product, they would have included Step A under the rubric manufacturing.
Q. Okay. But now I'm asking about specific instances that you may recall.
A. I think that I've been through this hierarchical characterization before. We worked with this kind of concept as part of the design methodology management projects at MCC, for example.
Q. You did design methodology management?
A. Yes.
Q. Was that -- was that the term that was applied to the program or --
A. We had an effort that was attempting to understand the methodology people used to create products from beginning to end, and we called it design methodology management. But if you had -- what we were dealing with were the steps that

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you went through to the manufacture of a product.
So, again, you're trying to, for some reason, in some way, draw a distinction between two things that clearly overlap in everybody of this art's minds, and there's just -- I don't -- as I've said a number of times, I don't even understand trying to make that distinction.
There are things that people might, in some context, call design. There's things that in some kind of context people say it's manufacturing. But if you look at what is called the manufacture of an ASIC, all of those steps fit together as being part of what's necessary to be done to manufacture that ASIC product.
Q. But you've described certain things that would be more design oriented than -- than other things and so on. What I'm wondering is there a continuum here? If one -- Can we start at these higher levels that "A" and "B" are more designed oriented and things later on in the process are more manufacturing oriented? Is it continuum, or are they -- I think you said they weren't synonyms. Are they synonyms of each other?
A. I don't think -- I don't think I said that before. Now that you've asked me, I wouldn't think of them as being totally synonymous.
But I've given you a couple of points. First, I said that someone can apply the term "design" to almost

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every one of these steps, if not all of them. Now, what people might say in a casual sense is one thing; but what people would understand to be the process of manufacturing a circuit -- an ASIC in a legal context or in a formal context is different. And I believe, if asked the question what are the essential steps in manufacturing an ASIC product, that this is a reasonable answer. I think that it would be an answer that would be understood and not disagreed with by the people in the field.
Q. Okay. Now I want to focus on actual conversations that you recall, if you recall any. And my question is do you recall anyone using the word "manufacturing" to describe something that they did that would fall within the scope of 10(A)?
A. I don't have any recollection of ever trying to apply the term "manufacturing" individually to these -- to that early step, no. I don't have -- I can't say I haven't, but I don't have any recollection of that.
Q. Okay. I'll ask the same question about 10(B). Do recall any instance where someone doing something that would fit within the scope of 10(B) referred to what they were doing as manufacturing?
A. I think that they would -- you know, I don't have any specific recollection of any conversation with anybody. That's the answer to the question. Either way, I don't have a

recollection of having such a conversation.

Q. Do you have any -- Are you familiar with any articles in textbooks that would use -- that you could point to to say that they used manufacturing to refer to something in the scope of 10(A) or 10(B)?

A. I come back to the original answer I gave you. If people were attempting to define -- and I haven't searched my textbook library or the Internet or anything to try to confirm your question. But I think people would understand that these are steps, all of them, "A" through "G," that are part of the manufacturing process. If the question is asked in that way, I think that then people would say, "Yeah, that's a step in the manufacturing process." Did they ever call individually Step C manufacturing an ASIC, I don't recall either way that anybody does that. And I can't cite to you any dictionary definition or textbooks that would say either way. I've never studied it. I don't know.

Q. And the same is true for 10(A) and/or 10(B); you can't cite any textbooks or definitions or articles that -- that would call those manufacturing?

A. Well, in part, that is because I've made no effort to find any such citations --

Q. Sure.

A. -- and so I'm unprepared to give you an answer.

Q. Okay.

A. That's not a negative answer. It's an answer that says that I haven't looked for those.

Q. Understood.

Did you -- You say you looked at the patent. Did you look at the patent to see how it used words -- words that are used that are described in the patent?

MS. ALLEN: Objection. I think you need to point to exactly what you're talking about because I think it's vague.

A. I think the answer is no. I read the patent. I read the file history. I looked at the -- at the claims at one time probably six or seven months ago. But in preparing the steps in Paragraph 10, I did that independently of any statements that were made in the patent.

Q. I'm going to ask you a couple of questions. I'm going to make a formal statement. It may or may not be helpful. One of the things that the Court may want to look at is the Court -- is whether something is used directly in manufacturing or indirectly in manufacturing. I've been talking about questions that are an attempt to get at that question.

Do you understand any distinction between saying that something is used to directly manufacture or something is used indirectly in manufacturing?

A. I don't understand the context of that statement. I

don't understand that concept at all.

Q. So if it became important in the resolution of some issue before the Court as to whether something is used directly in manufacturing or indirectly in manufacturing, would you have -- would you have any opinion on that?

MS. ALLEN: Objection. The question is vague. It calls for speculation.

A. I'd have to understand the context of the question the Court is trying to resolve, and I don't have enough context now to know what distinction the Court may be trying to make between directly and indirectly. I don't have enough background to answer.

Q. Okay. Do you -- is it true that the steps in "A" through "G" are -- some of them are more close in time to the actual formation of the ASIC at the foundry than other steps?

MS. ALLEN: Objection; vague and compound.

A. Well, they build upon top of each other. If it were a pure process where you did Step A and stopped doing "A" and then did Step B and didn't go back and reconsider Step A in this hierarchical flow of -- this cursory flow, then -- then you would expect these to be performed chronologically in sequence. So the latter steps would be closer to the actual manufacture than the earlier steps. By their nature, you wouldn't have the results of the earlier step to do the -- you can't do Step B until you've done Step A. So you have to do

"A" first. They -- they all flow together. I keep saying they're essential. You have to do them all in order to reach the end of the process.

Q. Okay. And am I -- It sounded like you were saying that in order to do Step G, I have to have done Step F, and in order to do Step F, I have to have done Step E, and likewise all of the way back up to Step A. Is that correct?

A. Yes. That's my -- that's my view of how these steps flow. Now, you may -- as I say, you may go back up. There may be reverse flows in the process where what you get when you try to do Step E forces you to do something that may be all of the way back up to even Step A. But if you take it as a one-way flow, then, yes, you have to do the previous step to get the results. I mentioned this hierarchy of representations. The representation you get at the end of one step is used as the representation for the next step.

Q. Okay. So then am I correct in assuming that if we're talking about the next step -- you don't say anything about the foundry right now and it being produced. Step A is going to be the most remote in time in terms of if I look at when -- when the last time I did it, Step A would be the one that happened furthest away back in the past. Is that correct?

MS. ALLEN: Objection; vague and compound.

A. As long as one -- and I think I've already answered

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that. As long as those steps are considered to be performed in a sequence and not recursed, then that would be true.

Q. But even if they are recursed, I'm still going to go back and do all of the steps that fell after -- after the step that was recursed. Is that correct?

A. I think there might be ways that you could go back and maybe even skip a step, if you were clever enough, when you're trying to make a late modification to the design for some purpose. You don't necessarily have to do every one.

You know, I don't -- It's probably better just to not offer you an answer on that. I'd have to look at a particular design flow and exactly what happened to know whether somebody did it formally or just sort of fixed it at the end. It's hard to say.

Q. Well, sitting here today, are you aware of any way you could go back to doing logic synthesis at Step B and not do Step C, Step D, Step E, Step F and Step G?

A. I don't really have an answer for that. I mean, that's -- someone may -- I don't have an answer to that.

Q. So you don't -- you don't know whether they could, and you don't know if they couldn't?

A. I don't know whether they might find some way to make a change in the -- in the top-level functionality and implement that directly by modifying the netlist without doing anything else.

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I think that could be done. As to whether I've ever actually done it myself, probably I've made some late design fixes almost at the mask level in the early days. But without clearly understanding -- I would understand that this had an effect on the functionality. I might even have gone back and run Step A to do a function resimulation. But I'm not sure I always did all of those steps late in the design review process. But in terms of it, I had to do them all at least in the initial flow. Beyond that, I'm not -- I don't really have a solid answer to give you.

Q. That would be a somewhat unusual flow, to go all of the way back up to logic synthesis and not to Step C, D, E, F and G. Is that correct?

A. I think it would be unusual not to flow through the process. That is correct. I'm just telling you there may be ways to shortcut it late in the game, but that would be the exception. And I'm not even sure I can cite to you a specific example. But as a manager, I wouldn't want that to happen.

Q. We had -- we talked about tapeout earlier. Does tapeout fit between one of these steps or maybe after these steps in "A" through "G"? What is the relationship between tapeout in these steps?

MS. ALLEN: Objection; compound.

Q. Well, let's just try the last question. What is the relationship between tapeout in these Steps A through G?

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A. Well, it would be late, and it could be between step -- at least in my personal experience, it would be between Step F and Step G --

Q. Okay.

A. The tape would contain the geometric data designing the physical layout in a manner that the masks could be created.

Q. And is it common for the folks who are doing Step G to be different than the steps doing -- the folks doing Steps A through F?

A. You already asked me that, and I think that might vary depending on time frame.

Q. All right. Let's talk about the present.

MS. ALLEN: You don't need to speculate.

A. Well, I wouldn't be speculating.

I think today, at least based on my experience at Motorola and other related semiconductor companies, it would be uncommon for the same person to do Step A and do Step G, for example.

Q. Okay. What about in the late '80s?

A. I think that would depend, to some degree, on the complexity of the device being manufactured. The same person, in those days, might have done everything in "A" through "F." I knew people who were also knowledgeable about mask fabrication who could have easily sat down and done Step A.

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But I don't know that that's true today because the mask technology has become so much more complicated.

Q. Was that common, though, back even in the late '80s, for someone -- an individual to do all of Steps A through G?

A. I would think even then it would be uncommon --

Q. Who are the --

A. -- at least for an ASIC of significance, I might say. Even that term has varied over the years. But it would -- unless the ASIC were particularly simple and the process were particularly simple, they would not.

Q. And we touched on this earlier, but the origin of the phrase "tapeout" is what?

A. I think it dates back -- My recollection is it dates to the magnetic tape that was produced, say, at the output of one of those machines when somebody had a magnetic tape in their hand and they passed it to the next stage in the manufacturing process.

Q. And why were -- why were they putting it on a magnetic tape? What was the rationale for putting it on a magnetic tape?

A. To move it to the next facility that was going to be doing the manufacturing.

Q. So, generally, Step G would have been performed at a different facility than the earlier steps. Is that correct?

A. It could have all --

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MS. ALLEN: Objection; foundation.
A. It could have all been in the same company, but it would take -- they'd refer to that like maybe as a mask shop would be the place where the photographic processes were done to make what they radicals. The images that were produced at that time were on glass. You would go -- It's very much like you would go into a photographic darkroom to make a print. So you had to -- But I think that same concept is applicable, really, in a sense between any of these steps.
Q. Well, is it called -- I mean, what -- is it being called tapeout because I'm taping it out, or how does -- where does the "out" part come from?
A. I just think it was an output. They produced the tape as an output at that stage of the process. But I think -- my experience is that you had tapes if one were far enough back in the magnetic tape domain, as opposed to, say, transmitting it through the Internet or something today, that you would produce representations that could have been represented on a magnetic tape or floppy disks or something between any of these steps.
Q. That was --
A. Computer readable representations could have been produced.
Q. And I take it that was, in part, sort of part of the purpose of the work that you're doing at MIC, to have these

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interfaces with -- in different points in the design process. Is that correct?
A. MCC.
Q. I'm sorry.
A. No, no problem. MIC is another one. I have no problem with that.
Yes. We were trying to come up with standardized representations and databases that could store and allow easy retrieval of those representations so that those sequence of representations could be passed from tool to tool in a way that you didn't have to go in and write a lot of data reorganization software, which had been the prior art.
In those days, each tool often had its own input and output format, and it would be incompatible with another tool from another vendor. So if you took the output representation from one vendor, you had to go through a rework process to convert it.
MS. ALLEN: Can we go off the record for one second.
MR. KELLEY: Sure.
(RECESS TAKEN)
MR. KELLEY: Back on the record.
Q. (Mr. Kelley continuing) Have you ever seen -- Have you ever heard anyone use the term "tapeout" to describe any of these -- you know, either the passage of data from one step

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to another in Steps A through -- between Steps A through F?
A. No.
Q. So there was a similar concept that could be -- that worked, but that term wasn't applied?
A. The simple answer is that term -- No. That was my answer. No, I haven't heard of it.
Q. Okay. I'll take it.
Have you ever worked in an area that touched on artificial intelligence or expert systems?
A. Yes.
Q. What was -- what was that?
A. Well, MCC was a hotbed of that technology from the time I went all of the way through. And the last three years that I was there, I managed a group that was focused on expert systems and neural maps and those kinds of AI technologies in various business applications. And when I -- I was working at -- earlier in the '80s up through the early '90s, we attempted to use some expert system technology to control sequencing through tools as a part of the -- that methodology management effort I was working on.
Q. What was the application of the later work?
A. There were lots of applications: Fraud detection on the use of like Visa cards; image detection like medical imaging; data mining, recognizing data relationships in large databases; transformation of Legacy databases to more modern

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formats; just general knowledge capture.
That's about the only things that I can recall. I'm sure there were some other applications that the people that were working under me were working on focus applications with those basic -- those basic technologies.
Q. Was any of that work related to CAD?
A. The earlier work that I mentioned of attempting to use expert -- the technology and methodology management was.
I'm trying to think if the later work would have been. I think by that time, the CAD program had pretty well -- the computer-aided design program had pretty well come to an end. That's one of the reasons that I was over managing the AI group. So I doubt if that had any direct relationship.
Q. Well, back in the earlier work when you were working with CAD and stuff, what kind of -- you know, what element of the program was -- involved artificial intelligence or expert systems?
A. I don't understand.
Q. Yeah. That's too general of a question.
Were you using a commercial expert system tool?
A. You know, I've thought of that. I think we looked at some commercial tools, and I'm not -- I don't even remember the names of them. But I think we basically took an inference engine that had been developed in a different part of MCC and used it to -- it and some support technologies to capture and

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run the rules that we were trying to exercise.
Q. Okay. And what is an inference engine?
A. Well, I think it's something that runs rules, that -- it evaluates expert rules.
Q. And what are rules?
A. Well --
MS. ALLEN: Objection. It's overly broad. Go ahead.
A. Well, again, I haven't addressed any kind of expert system context in my Declaration, and so I'm going to give you an answer that's totally outside of the context of the '432 patent.
Q. Sure.
A. Those are commonly some way of making, typically, an "if then" statement that some expert in a domain would understand and expressing that expert knowledge as a logical relationship.
Q. Okay. Is one of the functions of the inference engine to determine what rules to -- to evaluate or to apply?
MS. ALLEN: Again, objection. It's overly broad and outside the context of the Declaration --
A. I can't give you --
MS. ALLEN: -- outside the scope.
A. I can't give you a definite answer. I think that there are ways of writing the rules such that one rule can

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control the invocation of another rule. Sometimes that could be within the scope of what the inference engine does, and sometimes it wouldn't be. That's how I would characterize rules.
Q. What does the inference engine do other than identifying rules and applying rules?
MS. ALLEN: Again, objection. It's outside the scope of the Declaration and overly broad.
A. It just runs the rules and identifies the consequences that would -- against some current state, and it identifies the consequences of running those rules, and whatever those outputs from that are have to be implemented.
Q. Okay. The question that got us into this was whether you had used artificial intelligence or expert systems in your work, and we've talked now about expert systems.
Was there some other thing that might fall within the rubric of artificial intelligence other than expert systems that you have worked with?
A. In a CAD context?
Q. Yes.
MS. ALLEN: Again, it's outside the scope of the Declaration and overly broad.
A. I think the program may have been using some of that technology in some of their synthesis work, but I wasn't directly personally involved in either managing or

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contributing to that. So the answer is I don't have any personal experience at MCC in that other than the methodology management that I referred to earlier that I recall.
Q. Who worked up the first draft of your Declaration, Rhyne 1?
A. In terms of actually having it first typed, someone at Ms. Allen's law firm did. But it was based on some telephone conversations where I essentially narrated to them the steps that are shown in Paragraph 10. And in terms of the front information, I think that they took that, with some verbal modifications that I made during that phone call, from a previous report that I have done in another case.
Q. With regard to Paragraph 10, Steps A through G, did you break them down in this manner --
A. Yes.
Q. -- as "A" through "G" in this phone call?
A. Yes, I did. I essentially dictated those steps to them.
Q. Is there any reason that you didn't put in Step H at the time?
A. As --
MS. ALLEN: Objection to the whole mythical -- objection to the whole -- objection to foundation, I guess.
A. I understand the objection.
By Step H, you're referring to the final stages

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that would be done with the silicon. No. I think I told you earlier I just stopped at the point where the masks were available. There's no particular reason.
Q. So there was no particular reason why you stopped?
A. I don't think so. That's just what I said I thought were the essential steps. And you pointed out to me, and I agree with you, that it's certainly essential at the last part of the process to make one, but I just stopped there.
Q. Was the fact that you stopped with the mask data in any way related to the fact that the claims talked about mask data?
A. It may have been at the time, but I have no clear recollection. It's been months since I did this thing. I just thought when I went through it -- again, it's been months since I've dealt with the claims. So I can't tell you for sure that there's such a linkage, but I can't deny that that might have been part of why. I just don't remember.
Q. Were you trying to match up "A" through "G" with what was described in the subject matter of the patent and the claims thereof?
A. No. I told you that earlier. I really have not looked at the patent. So I think my recollection of the patent, at the point that we were doing this in February, was just in terms of its general applicability to the synthesis process to make the chip, and that's about all that was. I

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did not go back and review claims within the patent to try to match them at all.

MR. KELLEY: Okay. Why don't we take a brief break.

THE WITNESS: Okay.

(RECESS TAKEN)

Q. (Mr. Kelley continuing) Okay. So getting back to the Declaration, and I apologize if this -- I think this is a little bit different than what we talked about before, but I just want to make sure I understand.

In terms of these Steps 10(A) through (G), you're identifying, as you say, process steps that are an essential part of the manufacture of ASIC products.

Is there anything that one might characterize as design that falls after describing a series of the functions that are to be performed by the desired ASIC product manufactured that wouldn't be -- using your definition of "manufacturing" that you used here, wouldn't be appropriately also characterized as manufacturing?

MS. ALLEN: Objection; ambiguous.

A. I can't parse that statement.

Q. Okay. Let's break it down. I'm paraphrasing, but I think what you had said was that there was a lot of overlap between design and manufacturing, as you understood the terms and as you used them in your Declaration. Is that -- is that

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correct?

MS. ALLEN: Objection --

A. That's not really correct, no.

Q. Okay. Did you draw any distinction between design and manufacturing when you wrote this Declaration?

A. Every one of these steps, as I say in Paragraph 10's preamble, are an essential part of the manufacturing process. They're all manufacturing steps.

Q. Okay.

A. Now, you took me outside the context of this statement and said, "Well, you know, don't people refer to some of these stages as design," and I didn't disagree with you.

Q. Is there anything that -- that you're aware of -- Well, let me back -- try that question again.

Step A, I think, related to describing in some manner -- either using HDL or a spec or timing diagrams or something like that, describing the circuit to be designed in sufficient detail. Is that one? We specified its basic operation. Is that correct?

A. You said "circuit." I would prefer to say "ASIC," because circuit falls -- but the product, yes, that -- that is -- that's what I consider to be an essential first step. You have to --

Q. And once --

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A. -- describe what it's going to do.

Q. Once you've done that first step, is there anything that one might -- that folks might characterize as design that you wouldn't also say properly is included within the term "manufacturing"?

MS. ALLEN: Objection; vague.

A. Again, I don't understand. All of these terms -- all of these steps and terms, if you want to call them terms, fall within the terminology of manufacturing.

Q. The question I'm trying to get at is, setting aside these terms, is there something else that one might do after one has done Step A that would be characterized as design but not manufacturing?

MS. ALLEN: Objection; overly broad, vague, ambiguous.

A. You know, some day, Mr. Kelley, I hope we get an opportunity for you to explain to me what your real questions are here, because I've got tell you, as one of pretty good level of skill in this art, I don't even understand how to -- how to make this distinction. As clearly I've explained it to you, all I can do is restate it.

Every one of these steps are essential parts of the manufacture of the ASIC product. Some of them are commonly outside of that concept referred to as the design stages, but all of them are essential parts to manufacture the

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product. So all of them can be called manufacturing, and there's design associated with every one of them. So I don't know --

Q. Okay. But --

A. -- how to make that distinction.

Q. The question I'm trying to get at is are there things that could be called design that take place after Step A that you haven't mentioned here?

A. You asked me earlier --

MS. ALLEN: Objection; vague and ambiguous, overly broad.

A. You asked me earlier would -- you know, was this a complete list of every essential step, were there other steps. There may be. As I told you, I -- if you want to name something, and you tried two or three things on me like going out and buying the computers and -- so I can't give you an answer to that abstractly. There may be something.

But if it's essential as a step to eventually end up with the physical ASIC, then I think it's part of the manufacture. Whether you refer to that as also being something that could be characterized as design, it may be. I don't know.

These are the steps that came to mind when I was asked to list essential steps, and these are the ones that I have in mind. I don't have any others that I've held back.

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Q. Now, I think you -- I take it, then, that there is no step that's essential to a design that wouldn't also be essential to the manufacture of the ASIC. Is that correct?

MS. ALLEN: Objection; foundation, and it misstates prior testimony and is compound.

A. I think they just go hand-in-hand. Okay. You have to design it as part of the manufacture process. And so the -- in the context of the question I was asked, what are the steps -- the process steps that are an essential part of the manufacturing of an ASIC, these are steps that are both design and manufacturing, but they're all essential. You can't -- you can't leave one of these out and end up with an appropriate product at the end.

Q. Okay. So that sounded like a "yes," that there is -- that if anything is an essential design step, it's also an essential manufacturing step?

A. I haven't addressed the question of what is an essential design step whatsoever. I have no -- you've not asked -- you haven't used that -- that phrase, to the best of my knowledge, today. So I -- And the Declaration doesn't deal with whatever one might consider to be an essential design step. It deals only with an essential part of the manufacturing.

Q. But are you aware, sitting here today, of anything that might be required as a design step that you wouldn't also

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include as a manufacturing step?

A. Not --

MS. ALLEN: Objection; vague. It's, I think, outside the scope of the Declaration.

A. With -- within any of these steps, there's really substeps. I haven't attempted to lay out all of the process of logic synthesis or all of the process that one would go through in selecting components in the desired technology at this time.

So there are aspects of doing the steps shown in Paragraph 10 that are not specifically identified; but in terms of rolling them up into the top level, I think I've got everything here that -- that I think of when I was asked to lay out the essential steps in the manufacture.

Q. Understood. So I'm -- but I'm not getting at the question of whether -- you know, how much detail there is and is there more detail. Obviously, one can provide more detail.

What I'm asking you is there something -- sitting here today, are you aware of something that you would call an essential design step but say that's not part of the manufacture?

A. No. I'd have to -- but I'd be far more comfortable in giving you an answer if I was offered a candidate as to what that might be. It's kind of like when you asked me earlier could I provide you any references to books. It's a

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case of where I haven't thought about what one might try to identify. I feel that this is a complete and sufficient list. I think it's right. I don't think it's in error.

Q. You're not aware -- We said that admittedly we could add more detail to some of these things, but I'm not asking you about detail. You're not aware of a design step that's not included in here that's essential?

A. I think I've already answered that. I don't -- I don't have anything to add to this. I think it's as complete as I feel is appropriate for the purposes that it was intended.

Q. What is -- What is RTL?

MS. ALLEN: Objection. It's outside the scope of the Declaration.

A. It actually has two meanings, one that's not as common any more, which was resistor transistor logic.

Q. Right.

A. But I think in this context, it's register transfer logic. It's one form of representing the structural -- the structural design of a system. It also could be done in a language fashion. That are some RTL description languages.

Q. What distinguishes RTL from some other formats, some other -- what's characteristic of an RTL description --

MS. ALLEN: Objection --

Q. -- of a design?

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MS. ALLEN: Objection. It's outside the scope of the Declaration. I think we're going to be getting into attorney/client work product, and I'd have to -- to the extent it's outside the Declaration and what the witness relied on to prepare the Declaration, I think it's something he shouldn't answer.

THE WITNESS: Are you directing me not to answer that question?

MS. ALLEN: I mean, if there's something in your Declaration that relies on that, fine. I'm not trying to keep that from Mr. Kelley. But other than that --

MR. KELLEY: Well, we talked about RTL earlier in the testimony, what RTL is --

MS. ALLEN: But to the extent his Declaration didn't rely on that or his opinions in the Declaration don't rely on the level of detail you're trying to get into, I think it's attorney/client product -- excuse me, attorney/client privilege or work product information.

MR. KELLEY: RTL is attorney/client work product?

MS. ALLEN: I think trying to get his opinions on it, to the extent they don't relate to the Declaration, is going too far, yes.

MR. KELLEY: I'm trying to ask him to define a term he used. I'm not going to argue with you anymore. You

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either instruct him not to answer or you don't. It's your call.

MS. ALLEN: Yes, I've instructed him not to answer.

Q. Are you not --

A. I'll follow that instruction.

Q. Real quick, can you explain to me your understanding of the term "RTL"?

MS. ALLEN: I have the same objection. I think he's given an answer, and that's as far as I think is appropriate to go.

THE WITNESS: So you're again directing me not to answer that question?

MS. ALLEN: Yes. The answer you've already given -- that you've already given is fine.

MR. KELLEY: He did not give me a definition of RTL. He hasn't. So if you're not going let him answer that, that's where we're going to be. I'm asking --

MS. ALLEN: That's where we are.

MR. KELLEY: Okay.

A. Now, I'm going to correct something. I did give you a definition of it. The question you asked me was a different question that had to do with what distinguished it from other forms, and that's the question that she's directed me not to answer. So your statement was incorrect.

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Q. I stand corrected. You are correct. I wanted you to expand on the definition.

A. I understand, and I've been directed not to do it and I won't.

Q. Okay. Can you tell me what cases you've worked on since 2000?

A. Probably not. I can provide you that information.

Q. Why don't we do it that way.

A. I can make -- I can make a stab at it, but I doubt if I will get them all.

Q. Why bother. I'd just like to get --

MS. ALLEN: I can give you his CV.

MR. KELLEY: Well, I want to know what he's worked on in the last couple of years.

A. My CV will not provide you that information. But I -- I have, as an example, a recent report -- a four-year kind of report with that stuff in it. Unless her firm directs me not to do it, I can certainly provide that to them and they to you.

Q. That's what I'd like. I'd like to see that and a copy of your most recent CV.

A. I wasn't aware that you had not been provided it.

MS. ALLEN: Well, we didn't have one, either, in connection with this litigation so...

MR. KELLEY: I think that's it. I think we're done.

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THE WITNESS: Thanks.

MS. ALLEN: I may have one or two questions, but I just need a minute to think about it.

MR. KELLEY: Okay.

MS. ALLEN: Oh, also, are you okay with him signing at home or wherever he is comfortable signing?

MR. KELLEY: Yes.

EXAMINATION

BY MS. ALLEN:

Q. Dr. Rhyne, I'd like to point you to Rhyne 1, which is your Declaration, Paragraph 10. It's Subparagraph D, "Producing a description of the circuit components as well as their respective connections in the form of a netlist."

Do you see that?

A. Yes.

Q. Would it be accurate to describe a netlist that is output as a result of that step as a tapeout? Could a netlist be described as a tapeout?

MR. KELLEY: Objection to the form of the question.

A. As I told Mr. Kelley earlier, it could be; although, I don't think that's a common use of the phrase "tapeout." But if it was produced on tape and is the next step in the process, it could be called tapeout.

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Q. Thank you.

A. Certainly, in a design reference, tape is usually a computer readable form.

MS. ALLEN: No further questions.

MR. KELLEY: I have one.

FURTHER EXAMINATION

BY MR. KELLEY:

Q. I just want to confirm that you've never heard anyone use that term to refer to the output or Step D, have you?

A. If I were an attorney, I would say "asked and answered." But the answer is again -- and I'll make you happy, Mr. Kelley, is I have not heard that term used as tapeout at that stage.

Q. Thank you very much.

A. All right. Thanks.

WITNESS' CORRECTIONS AND SIGNATURE

Please indicate changes on this sheet of paper, giving the change, page number, line number and reason for the change. Please sign each page of the changes.

The reason for making changes are:

(1) To clarify the record;
(2) To conform to the facts;
(3) To correct transcription errors.

PAGE/LINE	CORRECTION	REASON FOR CHANGE

I, V. THOMAS RHYNE, have read the foregoing deposition and hereby affix my signature that same is true and correct, except as noted above.

This _____ day of _____, 2004.

_____
V. THOMAS RHYNE

THE STATE OF _____)
COUNTY OF _____)

BEFORE ME, _____, on this day personally appeared V. THOMAS RHYNE, known to me (or proved to me under oath or through _____) (description of identity card or other document) to be the person whose name is subscribed to the foregoing instrument and acknowledge to me that they executed the same for the purposes and consideration therein expressed.

Given under my hand and seal of office this _____ day of _____, 2004.

_____
NOTARY PUBLIC IN AND FOR
STATE OF_____

My Commission Expires:
_____.

UNITED STATES DISTRICT COURT
NORTHERN DISTRICT OF CALIFORNIA
SAN FRANCISCO DIVISION

RICOH COMPANY, LTD., Plaintiff, vs. AEROFLEX, INCORPORATED, AMI SEMICONDUCTOR, INC., MATROX ELECTRONIC SYSTEMS, LTD., MATROX GRAPHICS, INC., MATROX INTERNATIONAL CORP., and MATROX TECH, INC., Defendants.

Case No. CV 03-04669 MJJ (EMC)

REPORTER'S CERTIFICATE
DEPOSITION OF V. THOMAS RHYNE
April 14, 2004

I, Kathleen Casey Collins, Certified Shorthand Reporter in and for the State of Texas, hereby certify to the following:

That the witness, V. THOMAS RHYNE, was duly sworn by the officer and that the transcript of the oral deposition is a true record of the testimony given by the witness;

That the deposition transcript was submitted on _____, 2004, to the witness or the attorney for the witness for examination, signature and return to me by _____, 2004;

That $_____ is the deposition officer's charges to the Defendants for preparing the original deposition transcript and any copies of exhibits;

I further certify that I am neither counsel for, related to, nor employed by any of the parties or attorneys in the action in which this proceeding was taken, and further that I am not financially or otherwise interested in the outcome of the action.

Further certification requirements will be certified to after they have occurred.

Certified to by me this _____ day of April, 2004.

_____
KATHLEEN CASEY COLLINS
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Expiration date: 12/31/04
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FURTHER CERTIFICATION

The original deposition was/was not returned to the deposition officer on _____;

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Attorneys for Ricoh Company, Ltd.

UNITED STATES DISTRICT COURT
NORTHERN DISTRICT OF CALIFORNIA
SAN FRANCISCO DIVISION

RICOH COMPANY, LTD, Plaintiff, vs. AEROFLEX, INC. ET AL. Defendants.	)	Case No. C03-4669 (Judge Jenkins) DECLARATION OF TAKAMITSU YAMADA

Takamitsu Yamada declares as follows:

1. My name is Takamitsu Yamada, and I am an Assistant Manager of Ricoh Company, Ltd ("Ricoh"). I am over the age of 21 and am competent to make this declaration. Based on my personal knowledge and information, I hereby declare to all the facts in this declaration.

2. As an Assistant Manager, I am responsible for managing steps involved in the manufacture of Application Specification Integrated Circuits ("ASICs"). The specific steps that I am involved in and aware of begin with the development of written specifications describing such ASICs and extend through to the production of a netlist of hardware cells (and the interconnection requirements therefore) which perform the intended functions of the manufactured ASIC, the creation of mask works from the netlist, and the fabrication of the ASIC using the mask works.

3. In my experience, a typical process used to manufacture an ASIC begins with the creation of a written specification describing the desired functions to be performed by the ASIC. Ricoh, for example, has written specifications for ASICs that Ricoh intends to sell to others. From the written specifications, circuit components (referred to as "hardware cells") and the interconnection requirements therefore are synthesized. The circuit components are selected so as to perform the functions and adhere to any limitations (referred to as "constraints") set forth in the written specifications.

4. As part of the ASIC manufacturing process, the synthesized hardware cells can then be optimized to produce a more efficient ASIC design. A verification step may also be performed on the ASIC design to verify that this optimized design performs the same functions as the pre-optimized design. The selected hardware cells, including any

optimized hardware cells, and the manner in which these cells are interconnected are provided in a netlist. Among the tools that Ricoh utilizes in carrying out this portion of the manufacturing process is the Synopsys Design Compiler Family of tools, HDL Compiler tools, VHDL Compiler tools, and the DesignWare/Building Block IP Family.

5. As the ASIC manufacturing process continues, the netlist is placed and routed. In other words, the netlist is fed into the next manufacturing tool for the layout (or placement) of the netlist hardware cells, one relative to another, in the ASIC. The paths of the interconnection requirements between these netlist cells are routed (e.g., the paths that the hardware cell interconnection requirements follow from one hardware cell to another is determined).

6. The inputted netlist, as placed and routed, is used in the next step in the manufacturing process to build a three-dimensional representation (referred to as a "mask"). In a further step in the manufacturing process, a prototype of the ASIC is fabricated according to the mask and tested. Once acceptable, the mask is utilized in the subsequent fabrication steps of the process of manufacturing the ASIC.

I declare under penalty of perjury under the laws of the United States of America that the foregoing is true and correct. Signed at Kanagawa, Japan on February 6, 2004.

Takamitsu Yamada

Takamitsu Yamada

IN THE UNITED STATES DISTRICT COURT
NORTHERN DISTRICT OF CALIFORNIA
SAN FRANCISCO DIVISION

RICOH COMPANY, LTD.,

Plaintiff,

v.

AEROFLEX INCORPORATED, AMI SEMICONDUCTOR, INC., MATROX ELECTRONIC SYSTEMS, LTD., MATROX ELECTRONIC SYSTEMS, LTD., MATROX GRAPHICS, INC., MATROX INTERNATIONAL CORP. and MATROX TECH., INC.,

Defendants.

No. CO3-04669 MJJ (EMC)

TRAVEL TRANSCRIPT

SYNOPSYS, INC.,

Plaintiff,

v.

RICOH COMPANY, LTD.,

Defendant.

No. C03-2289 MJJ (EMC)

DEPOSITION UPON ORAL EXAMINATION OF
ERIK OLSON

9:00 a.m.
August 2, 2005
CLARION SEA-TAC AIRPORT HOTEL
3000 South 176th Street
Seattle, Washington 98188

REPORTED BY: Judith A. Robinson, CCR #2171

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INDEX

SEATTLE, WASHINGTON; TUESDAY, AUGUST 2ND, 2005
9:00 A.M.
--oOo--
(Whereupon, The Declaration Of Erik Olson, Dated August 9, 2005 was marked Exhibit-53 for identification.)
ERIK OLSON, witness herein, having been duly sworn on oath was examined and testified as follows:

EXAMINATION

BY MS. ALLEN:

Q. Mr. Olson, can you please say and spell your name?
A. My name is Erik Olson; E-R-I-K, O-L-S-O-N.
Q. Can you state your address, please?
A. Yeah. 4510 167th Avenue Southeast, Issaquah, Washington.
Q. Is that your home?
A. Home address.
Q. Can you state your work address?
A. I have to look on my card but I can do that.
Q. Can you just state the city?
A. It's Bellevue, Washington.
Q. Tell me about your post high school educational background. Where did you go to school?
A. I went to the University of Minnesota on the Duluth campus.
Q. What did you study there?
A. Computer science and engineering.
Q. Did you receive degrees in either computer science and computer engineering?

A. Both.
Q. What kind of degree was it?
A. Bachelor of science degrees in both.
Q. When did you receive the bachelor of science in computer science?
A. Bachelor of science in computer science was 1988.
Q. What about computer engineering?
A. 1988.
Q. Okay. Was the bachelor of science the highest degree you attained?
A. That's correct.
Q. Did you do any post-graduate study?
A. No.
Q. Mr. Olson, I want to talk about your work experience.
Can you tell me what your current position is?
A. I'm a director of physical implementation engagements.
Q. What does a director of physical implementation engagements do?
A. I manage a small team of tool experts to help complete tool engagements for our sales team.
Q. And who is your employer?
A. My employer is Synopsys.
Q. You said you manage a small team. Is your

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position primarily managerial then?
A. That's correct. My position is management.
Q. Can you say for me one more time what a director of physical implementation engineering does?
MS. FINK: Objection. Asked and answered.
BY MS. ALLEN:
Q. She can read back the answer. It's up to you.
A. I have a small team of engineers that run tool engagements to help sell our tools.
Q. And what kind of tools are those?
A. What kind of tools do my team run specifically?
Q. Yes.
A. They run what's generally known as back end tools. Specifically, they run Physical Compiler and Astro.
Q. When you say, "tool engagements," what does, "tool engagements" mean?
A. Physical Compiler and Astro are commonly known as some of our tools we sell. When customers choose to look at our tools and look to purchase they evaluate. This is a presales trial of our tools.
Q. You said your role now is primary managerial. Have you ever in your career performed hands-on as your primary job function?
A. Yes, I have.
Q. Can you tell me about that?

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A. The last time I was directly responsible for hands-on tool engagements was 1997.
Q. Was that in the same area that you're currently managing?
A. No. It was not.
Q. Okay. What area was that?
MS. FINK: Objection. Vague and ambiguous as to area.
BY MS. ALLEN:
Q. Can you describe the work you were doing in 1997?
A. In 1997, I was an application consultant, supporting primarily the Design Compiler tool.
Q. All of this was work done for Synopsys as well?
A. That's correct.
Q. Now, you mentioned that your current position is located in Washington. Is that near the Seattle area where your current position is?
A. My current position is in Bellevue, Washington. That's near Seattle. That's correct.
Q. Is there a name for the facility located in Bellevue?
A. Commonly, it's known as The Summit. If you like, I can get my card in my briefcase and give you the address. I'm sorry. I don't have it memorized.
Q. What is done at The Summit? Are you comfortable with me calling it, "The Summit"?

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A. Sure.
Q. What kind of work is done at The Summit?
A. Do you mean Synopsys work in particular?
Q. Yes.
A. Synopsys has an office of about 15 people. And it's a mix of sales, support and a handful of R&D.
Q. Does your position fall under sales, support or R&D?
A. My position is in the support organization.
Q. Now, you mentioned that -- well, let me ask this: Are there other companies -- is The Summit a Synopsys facility or a general facility?
A. We lease space in The Summit.
Q. Now, the companies that lease space, are they companies that you work with in your job function? Or are they --
A. No. There's no companies I work with, aside from Synopsys that are also in this building.
Q. So these would be unrelated. I'm trying to figure out if they're unrelated.
A. They are unrelated.
Q. Okay. Now, the sales in R&D that's performed at The Summit location, are those also within the physical implementation engineering function or related to the physical implementation engineering function?
MS. FINK: Objection. Vague and ambiguous as to "related."
THE WITNESS: The sales operations in this office sell the physical implementation tools, as well as the rest of the Synopsys tool portfolio.
BY MS. ALLEN:
Q. And by, "physical implementation tools," you're referring to Physical Compiler tool and Astro; is that correct?
A. Yes. That's generally correct.
Q. Are there any other tools that you're referring to then as physical implementation engineering?
A. The only other tool that could be described as a physical implementation tool would be JupiterXT. It's also known as JXT.
Q. What is JupiterXT?
A. JupiterXT is a design planning tool.
Q. What is Astro?
A. Place and route tool.
Q. And Physical Compiler?
A. Physical Compiler is a physical synthesis tool.
Q. What do you mean by, "physical synthesis"?
A. It combines synthesis mainly and specifically, in this case, optimization and placement.

Q. I'm going to give you what has been premarked as Exhibit 53 and a copy for Ms. Fink as well. Yours is the one with the label on it, Mr. Olson.

Do you recognize what has been marked as Exhibit 53?

A. Yes. I recognize this.

Q. And can you tell me what this is?

A. This is a declaration that I did as asked by my company.

Q. Okay. And can you turn to page 2 of the declaration, paragraph one, where you describe yourself as director of applications consultant at Synopsys?

Now, is that the same as physical implementation engineering?

A. Physical implementation engineering is a group within the applications consulting group.

Q. Your position is limited to physical implementation engineering or are you a director of the overall consulting?

A. My position is limited to the physical implementation engagements.

Q. Can you describe for me what other areas of application consulting there are?

A. Uh-huh. The other areas of application consulting are verification of engagements. And there are regional

managers and then the regional management structures underneath those.

Q. But it would all be related to either physical implementation engineering and verification of --

A. No.

Q. Tell me what regional managers --

A. The regional managers own a particular geographic region.

Q. And can you tell me what -- you say they own a particular geographic region. What does that mean?

A. They are responsible for the support of customers in that geographic region.

Q. Is that for application consulting tools or other tools as well?

A. For all Synopsys tools.

Q. Okay. Are there -- so applications consulting is -- let me ask it this way:

Physical implementation engineering is under the umbrella of "Applications Consulting"?

A. That's correct.

Q. Now, is there any department or group under "Physical Implementation Engineering"?

A. No. There's not.

Q. Now, do you know if there's any department above "Applications Consulting"?

A. Yes. There are -- there is. Applications Consulting is part of a larger group called Worldwide Application Services.

Q. Can you describe for me what Worldwide Application Services does?

A. In simple terms, Worldwide Application Services is responsible for the support of customers of the Synopsys tools.

Q. And again, that would be all Synopsys tools?

A. That's correct.

Q. Mr. Olson, are you familiar with the term, ASIC?

A. The acronym, Application Specific Integrated Circuit.

Q. Can you tell me what an Application Specific Integrated Circuit is?

A. In general terms, an ASIC is a semi custom-designed, silicon-based circuit to perform a specialized function.

Q. Are you familiar with the term, logic synthesis?

A. I am familiar with that.

Q. Can you tell me a general description of what that means?

A. It means 2 things. It means translation from a higher level language description and then optimization.

Q. Are you familiar with computer-aided logic

synthesis tools?

MS. FINK: Objection. Vague and ambiguous as to what you mean by, "familiar with."

THE WITNESS: I'd like you to define that term, I guess.

BY MS. ALLEN:

Q. Are you familiar with Design Compiler?

A. Yes.

Q. What about HDL Verilog? V-E-R-I-L-O-G.

A. I am familiar with HDL Compiler for Verilog.

Q. What about VHDL Compiler?

A. Yes.

Q. These are all Synopsys tools?

A. These are all Synopsys tools. That's correct.

Q. I believe you mentioned earlier, that you had at least one job function that related to Design Compiler. But I'll ask the question:

Have you used Design Compiler in context with your work for Synopsys?

MS. FINK: Objection. Vague and ambiguous as to time.

BY MS. ALLEN:

Q. At any time, from the time you started at Synopsys?

A. From 1991 to '97, I supported and used Design

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Compiler.
Q. How about HDL for Verilog? Have you used that tool?
A. From 1991 to '97 I used that.
Q. What about VHDL Compiler?
A. Same time frame.
Q. When did you start working with Synopsys?
A. I was hired by Synopsys on August 12, 1991.
Q. What did you do before you started at Synopsys?
A. I was a design engineer at General Electric.
Q. Can you describe what your job function as a design engineer was at G.E.?
A. At G.E., when I was a design engineer, I designed hardware boards. I also worked with ASICs and FPGAs.
Q. Your work involve logic synthesis at that time?
A. No, it did not.
Q. Mr. Olson, in preparing your declaration Exhibit 53, did you review any documents?
A. No. I did not review any documents in preparing my declaration.
Q. Okay. So are you aware of the patent that's at issue in this case?
A. I'm only aware of it through my attorney.
Q. But you haven't read it or reviewed it?
A. I have never seen the patent that's at stake here.

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Q. And are you aware the Court gave a claim construction? In other words, an order giving definitions of what some of the terms in the patent meant?
A. I'm aware of the claim construction through my attorney.
Q. But you've never read the claim construction?
A. I have never read the claim construction.
Q. Okay. Let's talk more about Exhibit 53.
I want to ask you a little bit about paragraph 4 where you describe back end design steps.
Your current position with Synopsys, is that position related to back end design or something else?
A. My current position is as a manager for a small group of what could be termed as back end designers.
Q. Okay. Now, would you consider back end design to be part of the logic synthesis?
A. Back end design is a vague term. But I do not define that to be involved with logic synthesis.
Q. Is that because it hosts the optimization phase? I'm going back to your definition you gave of logic synthesis.
MS. FINK: Objection. Mischaracterizes his prior testimony.
BY MS. ALLEN:
Q. I believe you previously testified that logic

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synthesis involves translation and optimization. And if any of that is not correct, just tell me what you mean or what you intended. And so my question to you is:
Is back end design then something that happens after optimization?
A. Back end design happens after logic synthesis. Logic synthesis is translation, plus optimization.
Q. Now then, looking at your -- your declaration, Exhibit 53, paragraph 3 describes what you call front end design.
Now, in a process flow, does front end design then precede back end design?
A. In a typical ASIC design flow, front end design precedes back end design.
Q. Can you describe for me then what front end design is?
A. Front end design is a somewhat vague term. Typically, I understand it to mean to capture the functionality required in the ASIC or the design verification of that functionality and then logic synthesis of that description.
Q. Have you ever been responsible for front end design in your professional career?
A. The work I did at General Electric would generally be considered front end design. However, at that time we

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did not use logic synthesis and we created our descriptions by hand.
Q. So was it a manual front end design process?
A. At that time, that was the front end process. There was no such thing as logic synthesis.
Q. What about any of your work for Synopsys? Did that involve front end design work?
A. My job at Synopsys, from 1991 to '97, involved supporting front end design but not actually doing front end design.
Q. When you say, "supporting front end design," tell me what you mean.
A. Synopsys is a provider of EDA tools who sells these tools for customers. They use them to do the job tasks. They supported them and aid them in getting the design tasks done using the Synopsys tools.
Q. Now, what is the output of the front end design phase?
A. What are -- so there are typically more than one output of a front end design phase.
Q. What are the outputs of a front end design phase?
A. Typically, the outputs of a front end design phase as I understand it, would be a gate level netlist, potentially some test patterns, and timing requirements. It's typically captured in what's known as an SDC file.

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Q. Do you know what is done with the test patterns on the front end phase?
MS. FINK: Objection. Calls for speculation.
BY MS. ALLEN:
Q. Now, if you don't know, that's fine.
A. Typically, the test patterns are used when the chip is to be tested or verified.
Q. Is that part of front end design or part of another phase, the test org. verification of a chip? You mean the actual ASIC, don't you?
A. I think you need to restate the question. I don't understand.
Q. Let me just ask you this:
The testing and verification that you described, is that part of the front end design phase or part of a different phase?
A. As I understand, the testing and verification can mean many different things. The testing of the -- the -- the design can involve verifying the functions correctly. That's not really part of the design phase as such. It's more of an analysis phase.
Q. What about the timing? Is that also part of an analysis phase?
A. The timing requirements as captured in an SDC file are used for both design phases or implementation phase as

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it's sometimes referred to and analysis.
Q. You mentioned a gate level netlist. Can you describe what you mean by that?
A. I understand a gate level netlist is a description of hardware components and their connection.
Q. I asked you about paragraph 5 of Exhibit 53, your declaration. You gave a definition of a netlist where you state:
"I understand that the Court has defined a netlist as "a description of the hardware components (and their interconnections) needed to manufacturer the ASIC as used by subsequent processes, e.g., mask development, foundry, etc."
Where did you get that understanding from?
MS. FINK: Objection, to the extent it calls for attorney/client privilege information. So if you got that information from one of your attorneys, then you should not answer.
THE WITNESS: I guess that's privileged.
MS. ALLEN: Let me ask this:
Is Mr. Olson being offered as an expert witness?
MS. FINK: He's being offered as a fact witness.
MS. ALLEN: Okay.
BY MS. ALLEN:
Q. Regarding paragraph 5, you did not review the

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Court's claim order to come up with that understanding. Is that true?
A. I did not.
Q. Okay. I'm going to ask you about your familiarity with libraries that are used with Synopsys, logic Synopsys tools.
Are you familiar with the term, "technology library"?
MS. FINK: Objection. Vague and ambiguous as to what you mean by, "familiar with."
BY MS. ALLEN:
Q. Have you ever heard of the term, "technology library"?
A. I have heard of the term, "technology library" in context with the Synopsys Design Compiler.
Q. Do you know what a technology library is? If you don't, I'm not asking you to guess. I'm just asking if you know?
A. I understand your question. In terms of Synopsys Design Compilers, specifically, a technology library is a description of the functionality and timing of a library set from a particular foundry and/or ASIC vendor.
Q. Did you say, from a particular foundry or ASIC vendor? Does a foundry or ASIC vendor supply the ASIC library?

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A. Yes. A foundry or ASIC supplier would supply that technology library for logic synthesis.
Q. You mentioned you had heard the term in context with Design Compiler. Does Design Compiler use technology libraries?
A. Design Compiler uses a format commonly known as Liberty, to describe technology libraries that are used then in the logic synthesis step with Design Compiler.
Q. Do you have any understanding of how a Design Compiler uses technology libraries in --
MS. FINK: I'm going to object to this whole line of questioning as exceeding the scope of his declaration.
THE WITNESS: I'm not an expert. I do not understand exactly how this works.
BY MS. ALLEN:
Q. Okay. Do you understand why technology libraries is needed during the logic synthesis phase?
MS. FINK: Same objection.
THE WITNESS: Logic synthesis is translation, plus optimization. The library is the final result that is optimized and the output from it.
BY MS. ALLEN:
Q. When you say, "it's the final result and it's optimized in output," what do you mean by "output"?

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A. I'm sorry. I wasn't complete in my answer then. From the Design Compiler tool operation, the output is typically a gate level netlist comprised of the hardware components from that technology library, plus the method for their interconnection.

Q. Now, the netlist that is output that you just described, is that the same netlist that you refer to in Exhibit 53 as part of the front end designs at paragraph 3 subsection 4, "Synthesis of the Description Into a Netlist"?

A. Can you repeat that question?

Q. Sure. At paragraph 3, section 4, you also describe a netlist there.

Is that the -- the netlist you described -- is the netlist you described as being output from the Design Compiler, is that the same netlist that you're describing at paragraph 3 subpart 4, the netlist, the synthesis of the description into the netlist?

MS. FINK: Objection. Vague and ambiguous.

THE WITNESS: As I understand the question, what -- what you're asking is, if what I described as the output netlist from Design Compiler, if that's the same as --

BY MS. ALLEN:

Q. The front end design netlist?

A. The front end section, 3, 4, that would be

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correct. So Design Compiler specifically outputs in netlist. And in general terms, the front end design logic synthesis would also output in netlist.

Q. Okay. Now, this netlist that is output, is it then fed into the back end phase of design that you describe in your declaration?

MS. FINK: Objection. Calls for speculation. He doesn't know what the customers necessarily do with it.

BY MS. ALLEN:

Q. I'm not referring to a particular customer.

A. Right.

Q. But the process flow that you're describing in your declaration the back end design stats, does it receive -- does the back end design phase receive a netlist?

A. In general terms in the process I described in my declaration, the back end design phase generally starts with a gate level netlist. Typically, that's from a front end phase.

Q. And what is the output of the back end design phase that you describe in your declaration at paragraph 4?

A. As I describe in my declaration, the output of the -- the general term back end design is mask data.

Q. And what is mask data?

A. As I understand it, mask data is used by the mask generation machines to create photo mask.

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Q. Tell me what a photo mask is.

A. I'm not an expert on photo mask. But as I understand it, these are used in the silicon fabrication to construct the various layers of the ASIC.

Q. Have you ever heard the word, "tape out," or words, depending on how you spell it?

A. I have heard of the word or phrase, "tape out."

Q. Do you know what it is?

A. As I understand it, it's generally meant to be a handout point from a design team. Could be at any phase of the design to the next section of the design or phase of the design.

Q. So then, could a netlist be on a tape out or be handed off as a tape out?

A. Typically, the phrase, "tape out" is meant to signify when a design has completed a back end phase.

Q. So then would mask data be handed off in the form of a tape out?

A. Typically, for a tape out, that is communication of -- of geometric information mask data. That could be used to create mask data information. Typically the format is GDS2.

Q. It's typically in the form of GDS2. Does it typically contain mask data then?

A. As I understand the process, the GDS2 is then used

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by the -- the generators of the mask, what are called mask shops, to create the mask themselves.

Q. Let me make sure I understand. I'm not sure your answer responds to the question.

The GDS2, does that represent the mask data that --

MS. FINK: Objection. Asked and answered.

THE WITNESS: The GDS2 represents the geometric description of the design.

BY MS. ALLEN:

Q. Well, let me then ask this:

The back end design phase, you indicated the output of that was mask data?

A. The back end design phase typically ends with GDS2 and that is communicated to the people who are responsible for making the mask. It's not directly mask data.

Q. Is there any relationship between mask data and GDS2?

MS. FINK: Objection. Vague and ambiguous as to, "any relationship."

THE WITNESS: As I understand it, I'm not an expert in that. But the GDS2 is a process by the mask data shops, if you will, into the mask data that's used to create mask.

BY MS. ALLEN:

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Q. So is it your understanding, that the GDS2 is created before the mask data is generated or after?
A. My understanding is, the GDS2 is created before the mask data.
Q. How is the mask data handed off from the back end design phase?
MS. FINK: Objection. Calls for speculation.
THE WITNESS: The mask data is not handed off from the back end design phase.
BY MS. ALLEN:
Q. What's the next thing that happens to the mask data at the – after it's generated?
After the mask data is generated, what is the next thing that happens to it?
A. After the mask data is generated, it's then used to create the actual photo mask.
Q. Let's take a look at 7G, which is page 5 of your declaration.
A. (Witness complies.)
Q. Do you have any understanding of what equipment is used to make the photo mask?
A. I do not know specifically.
Q. Okay. Can you explain for me then what in your – in your declaration, Exhibit 53, paragraph 7G, it describes mask data preparation and it mentions used by electron beam

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machines to make the photo mask.
A. That's my general understanding of how photo masks are created.
Q. By using an electron beam machine?
A. My general understanding, is that's how the photo masks are created, yes.
Q. Now, do you have any understanding whether the mask data is provided to the electron beam machine, in order to make the photo mask?
MS. FINK: Objection, "provided to."
BY MS. ALLEN:
Q. Is it input into the electron beam machine?
A. I don't know.
Q. According to your declaration at paragraph 3, the front end design phase generates a netlist. Is that an accurate representation?
MS. FINK: Objection. The document speaks for itself.
THE WITNESS: The front end -- as I understand the front end design phase, one of the outputs would be a netlist.
BY MS. ALLEN:
Q. And that netlist is input to the back end design phase?
A. In general terms. Again, the term, "back end

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design" is somewhat vague.
Q. Just using your term in your declaration.
A. Generally, the netlist is handed over and communicated to the back end design team of the phase and used for subsequent steps.
Q. Okay. And as a result of the back end design phase, mask data is generated?
A. That's not correct.
Q. So in your declaration where it describes the back end phase in the last step, there is generation of mask data, can you explain?
A. Yeah. Let me clarify. Typically, the output of the back end design phase is what's – it's a GDS2 file. That contains geometric information on various layers that are used. That information is then communicated to another phase of the design. Sometimes it's in – it could be loosely grouped with the back end where the mask data is created.
Q. So the back end design phase generates output this GDS2; is that correct?
A. That is typically correct.
Q. And after that, the mask data is generated?
A. That is -- as I understand it, that's correct --
Q. Okay.
A. -- with some additional processing steps.

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Q. Okay. Now, you mentioned earlier in your declaration at paragraph one, that you have been involved in the design of ASIC since 1989. You could go back and look up in paragraph one. I'm quoting from the third line, beginning with the words, "Involved in the design of ASIC since 1989."
Do you know whether in 1989, when you began being involved in ASIC, in the design of ASIC, do you know if people were using netlist to generate mask data or synthesis flow that involved generation of a netlist, which was later processed to generate mask data in the 1989 time frame?
MS. FINK: Objection. Vague and ambiguous and may call for speculation.
THE WITNESS: I think your question was -- there's 2 questions there.
BY MS. ALLEN:
Q. I can break it up.
A. Please.
Q. In 1989, do you know if there were synthesis process flows in which netlists were generated?
MS. FINK: Objection. Vague and ambiguous as to, "synthesis process flows."
BY MS. ALLEN:
Q. Do you not understand what I mean by, "synthesis process flows"?

A. My understanding in 1989, there were -- actually, I don't know. I don't know.
Q. So you don't know whether in 1989 people were generating that list as part of ASIC design processes?
A. Can you restate the question?
Q. Do you know whether in 1989, if people were generating netlist as part of ASIC design?
A. In 1989, people were using netlist as part of the ASIC design flow.
Q. Do you know whether in that 1989 time period, whether netlists were used in the generation of mask data?
MS. FINK: Objection. Vague and ambiguous as to, "used."
THE WITNESS: At that time?
BY MS. ALLEN:
Q. Do you not understand what I mean by "used"?
A. Netlist data can never be directly used to generate mask data.
Q. In the process flow. In other words, in a person designing an ASIC generating a netlist, the information in the netlist, do you know if it could be passed onto the next phase of the netlist, with the result being mask data generated?
A. Yes. At that time ASICs were, of course using masks to be created. And from a netlist standpoint people,

you know, could use netlists and do much subsequent processing to create the mask data prep.
Q. Okay.
A. That was one way of creating mask data information.
Q. Okay. Let's come back to your declaration.
Now, in just walking through this, after you've generated the mask data and it's handed off or passed on to the next phase of the process, the back end design, based on your testimony today, the output of that is generally GDS2?
A. The general -- in general terms, the output of back end design is GDS2.
Q. And in a next phase mask data is generated?
A. As I understand it, mask data is generated subsequent after a number of processing steps to the creation of the GDS2.
Q. And then the mask data is used to make the photo mask?
A. As I understand it, the mask data is used potentially with some processing to make the photo mask.
Q. And the photo masks are used to build up the ASIC layer-by-layer?
A. I'm not an expert in the actual manufacturing phase. But my general understanding is, the photo masks are used to create ASIC in the manufacturing phase.

Q. I'm going to ask you a little bit about your preparation for the deposition.
When were you -- when were you first contacted regarding your declaration?
A. I'm not clear of the day. But it was either late May or early June of this year I was contacted.
Q. Do you remember who contacted you?
MS. FINK: Objection, to the extent it calls for any disclosure of attorney/client privileged information. So any information communicated to you by Counsel you shouldn't answer, in terms of who contacted you at that time.
THE WITNESS: Let me see if I understand it.
MS. FINK: You can say who contacted you but don't say what they said.
THE WITNESS: Thank you. I was contacted by Erik Oliver.
BY MS. ALLEN:
Q. And Erik Oliver, can you tell me your understanding of who he is?
A. He's in some part of the synthesis legal department.
Q. Okay. I'm going to -- because I understand that you're claiming privilege. I need to make my record so I need to ask my questions. I'm not trying to sneak any

questions in on you. I'm forewarning you. I'm going to ask my questions.
Let me first have marked as the next exhibit. We're up to Exhibit 54.
(Whereupon, An Email From Erik Oliver To Erik Olson, Dated June 9, 2005 was marked Exhibit-54 for identification.)
BY MS. ALLEN:
Q. Do you recognize Exhibit 54?
A. I recognize it.
Q. Can you tell me what it is, please?
A. Exhibit 54 is an Email from Erik Oliver to me.
Q. Can you tell me the subject matter of the Email?
MS. FINK: Objection. The document speaks for itself.
THE WITNESS: The subject matter was a coworking session that was intended to create this declaration.
BY MS. ALLEN:
Q. Now, in the first line of the Email Mr. Oliver states:
"Thanks for helping out with this project."
Can you tell me what, "this project" is?
A. As I understand what he meant by this phrase, he meant this declaration.

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Q. You say a coworking session. Can you tell me who was involved in the coworking session?
A. The people involved in this session were myself, Erik Oliver, and I believe it was Terry. It might have been Jacky. Sorry.
Q. So either Terry Corbin or Jacky Fink?
A. And outside Counsel.
Q. When you say, "outside Counsel," are you referring to Ms. Fink and Ms. Corbin?
A. I think it was Ms. Fink.
Q. Okay. When he states, "We will VNC into my machine" and he gives what it looks like some sort of log-on or pass information, can you tell me what that means?
A. VNC is a -- is a technology that allows one computer user to see another computer user's desktop screen.
Q. So did you actually have had coworking session?
A. Yes. We had coworking session using VNC and a conference call.
Q. And during this coworking session using VNC, were you seeing what was going on on Mr. Oliver's machine or some person's machine?
A. During the session, he was viewing Erik Oliver's desktop screen and the work he was doing on that screen.
Q. Now, did this coworking session involve drafting your declaration?

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A. This session involved creating the declaration.
Q. So you did not actually type up your declaration yourself?
A. Erik Oliver typed up the declaration on his machine. I told Erik what, you know what to type up and what to say.
Q. So is the declaration all your words, or did some that come from someone else? You can look at it.
A. Most of the declaration are my words verbatim.
Q. Can you tell me what parts are not your words verbatim?
A. The parts I recognize as not my words verbatim are paragraph 5, the Court description. That pertains to the Court description. Again, I haven't seen any of the Court documents.
Q. Okay.
A. But this is a standard term, no --
Q. When you say, "this is a standard term," do you mean the definition?
A. Yes. I mean, standard definition for netlist.
Q. Okay. Anything else you recognize as not your words verbatim?
A. I don't recognize anything else in the declaration there that are not my words verbatim.
Q. So you -- did you then dictate this declaration as it exists here today during this coworking session that's described in Exhibit 54?

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A. Yes. I generally dictated this declaration during the coworking session.
Q. When you say, "generally dictated," what do you mean by "generally"?
A. During the coworking session, it was not -- it was a discussion. Of course, this did not come out of my mouth fully formed in this exact format.
Q. Okay. Let me ask this then:
Were there other meetings or sessions in which you did provide the language here, "fully formed," to use your term, as we see it here today?
A. I think what you're asking is, were there more sessions that we revised or improved that?
Q. You can answer that.
A. I believe we had one subsequent meeting to review the declaration one more time.
Q. You said most of these are your words verbatim?
A. Uh-huh.
Q. But then you said, you didn't dictate it to him. These are not your words, "fully formed"?
A. Sure.
Q. There's a disconnect for me there. If these were your words verbatim, tell me what that means.

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Do you mean you told him what to say and he typed it up? Or did you give him general topics and he flushed out language for you?
A. The working process for creating this declaration was, I gave him the general topics. We discussed what I meant by that. He asked clarifying questions. And then I provided and clarified the words in the sentences, the information.
Q. So the result of the coworking session that's described in Exhibit 54, at some point did you review a declaration that resulted from that coworking session?
A. I believe my recollection is that we did another coworking session on Erik's computer and reviewed the declaration.
Q. Now, the declaration that you reviewed that is part of that second coworking session on Erik's computer, is it identical to the declaration that you have here or were there changes made?
A. I -- I do not remember.
(Whereupon, An Email From Erik Oliver To Erik Olson, Dated June 14, 2005 was marked Exhibit-55 for identification.)
BY MS. ALLEN:
Q. Let's take a look at what has been marked Exhibit 55.

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Do you recognize Exhibit 55?
A. I recognize Exhibit 55.
Q. Can you tell me what it is?
A. It's an Email from Erik Oliver to Jacky and Terry and a courtesy copy to me.
Q. Can you tell me what the subject matter of Exhibit 55 is?
MS. FINK: Objection. The document speaks for itself.
THE WITNESS: The Email on Exhibit 55 states that Erik Olson is pasting and getting a final declaration signed.
BY MS. ALLEN:
Q. And the last paragraph is the one-sentence paragraph in Exhibit 55 and begins with the words, "ERIK OLSON."
Was that a message to you?
MS. FINK: Objection, speculation. The document speaks for itself.
BY MS. ALLEN:
Q. Did you understand that to be a message to you?
A. Yes.
Q. Can you tell me what you understood that message to be?
A. I understood from reading this Email that the

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team, I'm not sure who the team was, that we made some small changes since our -- since we had talked, I assume the first time in doing this coworking section. They would then send me the final version of the declaration on that date.
Q. How many of those coworking sessions were you involved in?
A. My recollection is not perfect. I remember the first one we spent a long time working on this declaration. We might have done one more. But my recollection is not clear on that.
Q. So does that mean at least 1, possibly 2?
A. It means for sure 1 and possibly 2.
Q. And that first coworking section, do you recall whether or not any of the language that we see here today in your current declaration was drafted then during that session?
A. If I understand your question correctly, what you're asking was, is any of the language that is in the declaration drafted on that first meeting? Is that correct?
Q. Uh-huh.
A. Yes.
Q. Yes. We both answered that at the same time. Yes to your question to me and you say yes.
Now, was it the declaration as we see it here? Or was it a draft form of the declaration that was drafted that

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first?
MS. FINK: Objection. Vague and ambiguous as to your description there.
BY MS. ALLEN:
Q. I'm just trying to clarify what was drafted during that first coworking session. It's not that final declaration we see here; is that correct?
MS. FINK: Objection. Mischaracterizes his prior testimony.
THE WITNESS: We did in the first coworking session the majority of the language that's captured in this declaration.
BY MS. ALLEN:
Q. Do you recall what was not captured during that first coworking section?
A. In terms of exact words, I do not recall. In terms of general ideas, everything that was in that first working draft is in this or first coworking session, I should say, is in this declaration.
MS. FINK: Could we take a break?
MS. ALLEN: Sure.
(Off the record.)
BY MS. ALLEN:
Q. A little earlier, Mr. Olson, we discussed you providing the address of the Synopsys facility where you're

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currently employed. Can you give us that address now?
A. Yes, I can. The address is, 10885 Northeast Fourth Street, Suite #200, Bellevue, Washington 98104.
Q. Can I ask you, do you know why that facility is located in Washington versus near Synopsys headquarters in Mountain View?
MS. FINK: Objection. Calls for speculation. I don't think he decided it should be there.
THE WITNESS: Synopsys, like many other software sales companies, has field sales offices near the customers. Primarily, this is a field sales office.
BY MS. ALLEN:
Q. Thank you. Now, just before the break, we were walking through the preparation of your declaration.
Take a step back for a moment to Exhibit 54, the Email from Erik Oliver to you regarding helping with the declaration project.
Was this Email your first communication regarding providing the declaration or did you have one before?
A. Specifically providing the declaration, I believe this is the first Email I have. Although, I'd have to review my records on that. I did get a phone call from Erik before he Emailed me.
Q. And did he tell you the nature of what he wanted during that phone call?

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MS. FINK: Objection, to the extent it calls for attorney/client privileged information. So you can answer yes or no.

THE WITNESS: Your question is, did he tell me -- can you restate the question, please?

BY MS. ALLEN:

Q. Well, let me ask you this:

What did he tell you during that phone call?

MS. FINK: Objection, to the extent it calls for attorney/client privileged information. You should not tell her what he said.

THE WITNESS: I guess that's privileged information.

BY MS. ALLEN:

Q. Can you tell me who participated in that first phone call?

MS. FINK: Objection. Asked and answered.

THE WITNESS: The first phone call was just myself and Erik Oliver.

BY MS. ALLEN:

Q. Can you tell me when your next communication regarding the declaration happened after the phone call?

A. The first communication after the declaration could working session.

Q. Well the next communication after the phone call?

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In other words when was the next time you were contacted or you contacted someone?

A. I don't know.

Q. Was there another communication after the phone call? Was there another communication between the first phone call and the Email that's Exhibit 54?

MS. FINK: Objection. Asked and answered. He said he doesn't remember.

THE WITNESS: I don't remember any other phone calls.

BY MS. ALLEN:

Q. No other types of communication?

A. The only other communication would have been setting up the meeting.

Q. Okay. And the meeting that's described in Exhibit 54, at this meeting you did not dictate the content of your declaration. Is that true? I want to understand you?

MS. FINK: Objection asked and answered.

THE WITNESS: In this coworking social that I had with Erik and Jacky, I did not type the declaration. Erik was working within Microsoft Word and typing the sentences as I stated the general flow that you see in the declaration.

BY MS. ALLEN:

Q. When you say as you stated, the general flow, did

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you state the sentences verbatim or general topics and Erik typed the sentences?

A. First, we went through the general steps that would constitute ASIC design process in loose terms. Then he divided that up into smaller steps. I think that would roughly translate to the paragraphs that you see here. And then we refined the sentences.

Q. Who came up with the term, "front end design"?

A. Who originally came up with that?

Q. As it worked its way into the declaration?

A. I don't remember. It's a very common term.

Q. You don't remember if it was you or someone else?

A. I don't remember if I introduced the term to the conversation or if Erik or Jacky did.

Q. Okay.

A. It's a commonplace term.

Q. What about the term, "back end design"? Do you remember who introduced that term into the conversation?

A. I do not remember who introduced that term into the conversation.

Q. During this first working session, did you take any notes at all?

A. I did not take any notes.

Q. Do you have any knowledge if anyone else did?

A. I have no knowledge of anyone else taking notes

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from this first working session.

Q. Okay. Do you remember whether you had a subsequent communication after this first working session? Any form of communication regarding the declaration?

A. In terms of communication, clearly yes. There's an Email in Exhibit 55.

Q. Was that the next communication you had after the coworking session?

A. I don't know if it was or not. I believe all the subsequent communication was done primarily through Email and all the Emails have been turned over. I would have to refer to the Emails to give you an exact answer.

Q. In Exhibit 55, the Email from Erik Oliver to you discussed, "We've made small changes since we talked. We'll get you the final sometime today."

You were not involved in the revisions or making those small changes; is that correct?

A. Again, my recollection isn't perfect on this. I believe that I had a phone call with Erik regarding some clarifications.

Q. Do you know what small changes he's referring to?

A. I don't know specifically what small changes he's referring to.

Q. Do you know whether or not you saw a draft of the declaration before the small changes were made?

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A. The way this document was created was primarily in the first working session, coworking section, I think is what we've been call it. We did all the work within the Microsoft Word environment. After that was completed, you know, that was the majority of the work done on the declaration.

Q. So the majority of the work was done on the declaration?

A. The majority of the work for the declaration or on the declaration was completed at that time is my recollection.

Q. The first coworking session?

A. Said another way, during the first coworking session, we created -- I created the majority of what you see in the declaration.

Q. When you say, "you created," tell me what you mean.

A. I mean I dictated it. When I say, "created," we went through the general flow of this process. We parsed it up into different paragraphs and refined sentences to clearly capture ideas.

Q. And the sentences in the declaration, are those your words or your general topics as Erik Oliver translated into his words?

MS. FINK: Objection. Asked and answered

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already.

THE WITNESS: The words in the document, I would say the vast majority are my words.

BY MS. ALLEN:

Q. Okay.

A. Erik might have suggested a different word here or there or corrected my grammar.

Q. During this coworking session, were you ever -- strike that.

During this coworking session, did anyone ever tell you what should be included in the declaration?

MS. FINK: Objection, to the extent it calls for attorney/client privileged information. You can answer yes or no. That's all. Or I don't know.

THE WITNESS: I don't know.

BY MS. ALLEN:

Q. In any of your communications, in addition to this first coworking session, did anyone ever tell you what should be included in the declaration?

MS. FINK: Same objection.

THE WITNESS: I don't know.

BY MS. ALLEN:

Q. Okay. During any of your communications regarding your declaration, did you take any notes?

A. I -- as I answered before, I took no notes during

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any of the communications.

Q. Do you have any knowledge of anyone else taking notes during any of the communications?

A. I have no knowledge of anyone taking any notes during the communications.

Q. Okay. Do you know if anyone other than you reviewed the declaration after it was finalized?

A. I have no knowledge of anyone else. I don't know.

Q. Do you have any knowledge of any drafts that are not identical to the one you signed existing?

A. No.

Q. Are you aware of a company called, Aeroflex, Inc.?

A. I am aware of Aeroflex.

Q. Have you ever met or communicated with anyone acting on behalf of Aeroflex, Inc., in connection with your declaration?

A. I have not met with anyone representing Aeroflex under any circumstances.

Q. Under no circumstances, declaration or otherwise?

A. That's correct.

Q. What about AMI Semiconductor? Have you heard of them?

A. Yes.

Q. Have you ever communicated with anyone acting on behalf of AMI Semiconductor, in connection with your

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declaration?

A. No.

Q. In connection with anything related to this litigation?

A. No.

Q. What about Matrox Electronic System? Have you ever heard of them?

A. I have heard of Matrox.

Q. There are a whole series of Matrox companies. I can go through each one of them. But I'll tell you which ones they are. In addition to Matrox Electronics, there's Matrox Graphics, Matrox International and Matrox Tech.

Do you group them under the umbrella, Matrox?

A. I have heard of them grouped under Matrox. I haven't heard of each of these individual companies.

Q. Have you ever heard of any discussions with anyone representing any Matrox entity?

A. No.

Q. Regarding this declaration or otherwise?

A. No.

MS. FINK: Objection. Asked and answered.

BY MS. ALLEN:

Q. Did you study or review the ASIC processes or any Matrox entity for your declaration?

A. I did not.

Q. Did you study or review the ASIC design processes of Aeroflex, Inc. in preparation for your declaration?
A. I did not.
Q. Did you study or review the ASIC design of AMI Semiconductor in preparation for your declaration?
A. I did not.
Q. Have you had discussions with anyone other than your attorneys regarding your declaration?
A. Yes.
Q. Can you tell me who that is or who those people are?
A. I discussed this -- the fact that I was doing this declaration with my direct manager, Deidre Hanford. We did not discuss any of the content or anything around that.
Q. Did Ms. Hanford review the declaration, to your knowledge?
A. She did not, to my knowledge, review the declaration.
Q. Was Ms. Hanford involved in the declaration, to your knowledge?
A. She was not involved in the declaration, to my knowledge.
Q. Did you discuss the declaration with anyone else, other than Ms. Hanford and your attorneys?
A. Not that I remember.

Q. And were your discussions with Ms. Hanford limited to the fact that you were doing a declaration and that's no content of the subject matter of the declaration?
MS. FINK: Objection. Asked and answered.
THE WITNESS: That's correct. I informed her I was doing the declaration and we did not discuss the content at all.
BY MS. ALLEN:
Q. Did you tell her anything else about the declaration, other than you were going to do one?
A. Not about the declaration specifically, no.
Q. How about anything else related to your work on this declaration project?
A. Not that I recall.
Q. Did you consult any documents in preparation of the declaration?
A. I did not consult any documents in preparation for this declaration.
Q. Were any documents provided to you?
A. No documents were provided to me for this declaration.
Q. Did you know if you received a subpoena in connection with your papers here today?
A. I did receive one.
Q. Did you review the subpoena?

A. I glanced at the subpoena.
Q. Did you understand the subpoena to be requesting that you turn over any documents or things as listed in the --
A. I didn't understand that the subpoena was requesting all documents related to this.
Q. And you had none to provide?
A. I had none to provide, except for the exhibit or declaration, Exhibit 53.
MS. ALLEN: Can we take a break for about 2 minutes?
(Off the record.)
BY MS. ALLEN:
Q. Mr. Olson, when you said you communicated with Ms. Hanford, how did that communication take place? Was it in person?
A. Phone call. We communicated via phone call.
MS. ALLEN: I have no more questions for Mr. Olson. I think we have differences about attorney/client privilege issues. But I have no more questions at this time.
THE WITNESS: Okay.
(Whereupon, the deposition of Erik Olson was concluded at 11:30 a.m.)

SIGNATURE

I declare under penalty of perjury under the laws of the State of Washington that I have read my within deposition. And the same is true and accurate, save and except for changes and/or corrections, if any, as indicated by me on the change sheet page hereof.
Signed in ....., Washington, on the ..... Day of ....., 2005.

_____
Erik Olson
Taken: August 2, 2005

Judith A. Robinson, CCR

CERTIFICATE

STATE OF WASHINGTON)
COUNTY OF KING) ss.
)

I, Judith A. Robinson, Certified Court Reporter and an officer of the Court under my commission as a Notary Public for the State of Washington, hereby certify that the foregoing deposition upon oral examination of said witness was transcribed under my direction;

That the witness was duly sworn by me to testify truthfully; that the transcript of the deposition is a full, true, and correct transcript to the best of my ability; that I am neither attorney for, nor a relative or employee of any of the parties to the action or any attorney or Counsel employed by the parties hereto, nor financially interested in its outcome.

IN WITNESS WHEREOF, I have hereunto set my hand and seal.

_____
NOTARY PUBLIC in and for the
State of Washington, residing
in Seattle.
My Commission expires November 4,
2008, CCR License #2171.

Preface

This preface includes the following sections:

- What's New in This Release
- About This Manual
- Customer Support

4

Working With Libraries

This chapter presents basic library information. Design Compiler uses technology, symbol, and synthetic or DesignWare libraries to implement synthesis and to display synthesis results graphically. You must know how to carry out a few simple library commands so that Design Compiler uses the library data correctly.

This chapter contains the following sections:

- Selecting a Semiconductor Vendor
- Understanding the Library Requirements
- Specifying Libraries
- Loading Libraries
- Listing Libraries
- Reporting Library Contents

- Specifying Library Objects
- Directing Library Cell Usage
- Removing Libraries From Memory
- Saving Libraries

Selecting a Semiconductor Vendor

One of the first things you must do when designing a chip is to select the semiconductor vendor and technology you want to use. Consider the following issues during the selection process:

- Maximum frequency of operation
- Physical restrictions
- Power restrictions
- Packaging restrictions
- Clock tree implementation
- Floorplanning
- Back-annotation support
- Design support for libraries, megacells, and RAMs
- Available cores
- Available test methods and scan styles

Understanding the Library Requirements

Design Compiler uses these libraries:

- Technology libraries
- Symbol libraries
- DesignWare libraries

This section describes these libraries.

Technology Libraries

Technology libraries contain information about the characteristics and functions of each cell provided in a semiconductor vendor's library. Semiconductor vendors maintain and distribute the technology libraries.

Cell characteristics include information such as cell names, pin names, area, delay arcs, and pin loading. The technology library also defines the conditions that must be met for a functional design (for example, the maximum transition time for nets). These conditions are called design rule constraints.

In addition to cell information and design rule constraints, technology libraries specify the operating conditions and wire load models specific to that technology.

Design Compiler requires the technology libraries to be in .db format. In most cases, your semiconductor vendor provides you with .db formatted libraries. If you are provided with only library source code, see the Library Compiler documentation for information about generating technology libraries.

Design Compiler uses technology libraries for these purposes:

- Implementing the design function

  The technology libraries that Design Compiler maps to during optimization are called target libraries. The target libraries contain the cells used to generate the netlist and definitions for the design's operating conditions.

The target libraries that are used to compile or translate a design become the local link libraries for the design. Design Compiler saves this information in the design's `local_link_library` attribute. For information about attributes, see "Working With Attributes" on page 5-51.

- Resolving cell references

  The technology libraries that Design Compiler uses to resolve cell references are called link libraries. In addition to technology libraries, link libraries can also include design files. The link libraries contain the descriptions of cells (library cells as well as subdesigns) in a mapped netlist.

  Link libraries include both local link libraries (`local_link_library` attribute) and system link libraries (`link_library` variable).

  For more information about resolving references, see "Linking Designs" on page 5-14.

- Calculating timing values and path delays

  The link libraries define the delay models that are used to calculate timing values and path delays. For information about the various delay models, see the Library Compiler documentation.

- Calculating power consumed

  For information about calculating power consumption, see the *Power Compiler Reference Manual*.

Symbol Libraries

Symbol libraries contain definitions of the graphic symbols that represent library cells in the design schematics. Semiconductor vendors maintain and distribute the symbol libraries.

Design Compiler uses symbol libraries to generate the design schematic. You must use Design Vision or Design Analyzer to view the design schematic.

When you generate the design schematic, Design Compiler performs a one-to-one mapping of cells in the netlist to cells in the symbol library.

DesignWare Libraries

A DesignWare library is a collection of reusable circuit-design building blocks (components) that are tightly integrated into the Synopsys synthesis environment.

DesignWare components that implement many of the built-in HDL operators are provided by Synopsys. These operators include +, -, *, <, >, <=, >=, and the operations defined by if and case statements.

You can develop additional DesignWare libraries at your site by using DesignWare Developer, or you can license DesignWare libraries from Synopsys or from third parties. To use licensed DesignWare components, you need a license key.

Specifying Libraries

You use dc_shell variables to specify the libraries used by Design Compiler. Table 4-1 lists the variables for each library type as well as the typical file extension for the library.

Table 4-1 Library Variables

Library type	Variable	Default	File extension
Target library	target_library	{"your_library.db"}	.db
Link library	link_library	{"*", "your_library.db"}	.db
Symbol library	symbol_library	{"your_library.sdb"}	.sdb
DesignWare library	synthetic_library,	{}	.sldb

Using a Library Search Path

You can specify the library location by using either the complete path or only the file name. If you specify only the file name, Design Compiler uses the search path defined in the `search_path` variable to locate the library files. By default, the search path includes the current working directory and $SYNOPSYS/libraries/syn. Design Compiler looks for the library files, starting with the leftmost directory specified in the `search_path` variable, and uses the first matching library file it finds.

For example, assume that you have technology libraries named my_lib.db in both the lib directory and the vhdl directory. If the search path contains (in order) the lib directory, the vhdl directory, and the default search path, Design Compiler uses the my_lib.db file found in the lib directory, because it encounters the lib directory first.

You can use the `which` command to see which library files Design Compiler finds (in order).

```
dc_shell> which my_lib.db
{"/usr/lib/my_lib.db", "/usr/vhdl/my_lib.db"}
```

Specifying Technology Libraries

To specify technology libraries, you must specify the target library and link library.

Design Compiler uses the target library to build a circuit. During mapping, Design Compiler selects functionally correct gates from the target library. It also calculates the timing of the circuit, using the vendor-supplied timing data for these gates.

You use the `target_library` variable to specify the target library.

The syntax for dcsh mode is

```
target_library = my_tech.db
```

The syntax for dctcl mode is

```
set target_library my_tech.db
```

Design Compiler uses the link library to resolve design references. You use the `link_library` variable to specify a list of libraries that Design Compiler can use to resolve design references.

The syntax for dcsh mode is

```
link_library = {* my_tech.db}
```

The syntax for dctcl mode is

```
set link library {* my tech.db}
```

Note that you specify the same value for the target library and the link library (except when you are performing technology translation). For the link library, you should also specify the asterisk character (*), which makes Design Compiler also search the designs in memory when it is resolving cell references. If the `link_library` variable has no asterisk, the designs loaded in memory are not searched. As a result, designs might not be found during linking and might be unresolved.

When Design Compiler attempts to locate a library file, it first searches the memory. Next, it searches the library files specified in the `link_library` variable and lastly, it searches the paths defined in the `search_path` variable.

When you specify the files in the `link_library` variable, consider that Design Compiler searches these files from left to right when it resolves references, and it stops searching when it finds a reference. If you specify the link library as `{"*" lsi_10k.db}`, the designs in memory are searched before the lsi_10k library.

For more information about resolving references, see "Linking Designs" on page 5-14.

Note that Design Compiler uses the first technology library found in the `link_library` variable as the main library. Design Compiler uses the main library to obtain default values and settings used in the absence of explicit specifications for operating conditions, wire load

selection group, wire load mode, and net delay calculation. Design Compiler obtains the following default values and settings from the main library:

- Unit definitions
- Operating conditions
- K-factors
- Wire load model selection
- Input and output voltage
- Timing ranges
- RC slew trip points
- Net transition time degradation tables

Note that if other libraries have units different from the main library units, Design Compiler converts all units to those that the main library uses.

Specifying DesignWare Libraries

You do not need to specify the standard synthetic library, standard.sldb, that implements the built-in HDL operators. The software automatically uses this library.

If you are using additional DesignWare libraries, you must specify these libraries by using the `synthetic_library` variable (for optimization purposes) and the `link_library` variable (for cell resolution purposes).

For more information about using DesignWare libraries, see the *DesignWare User Guide*.

Loading Libraries

Design Compiler uses binary libraries (.db format for technology libraries and .sdb format for symbol libraries) and automatically loads these libraries when needed.

If your library is not in the appropriate binary format, use the `read_lib` command to compile the library source. The `read_lib` command requires a Library-Compiler license.

To manually load a binary library, use the `read_file` command.

```
dc_shell> read_file my_lib.db
dc_shell> read_file my_lib.sdb
```

Listing Libraries

Design Compiler refers to a library loaded in memory by its name. The library statement in the library source defines the library name.

To list the names of the libraries loaded in memory, use the `list_libs` command.

```
dc_shell> list_libs
my_lib     my_symbol_lib
```

To list the path and file name information along with the names, use the `list -libraries` command (dcsh mode only).

```
dc_shell> list -libraries
Library          File          Path
-------          ----          ----
my_lib           my_lib.db     /synopsys/libraries
my_symbol_lib    my_lib.sdb    /synopsys/libraries
```

Reporting Library Contents

Use the `report_lib` command to report the contents of a library. The `report_lib` command can report the following data:

- Library units
- Operating conditions
- Wire load models
- Cells (including cell exclusions, preferences, and other attributes)

Specifying Library Objects

Library objects are the vendor-specific cells and their pins.

The Design Compiler naming convention for library objects is

`[file:]library/cell[/pin]`

file

The file name of a technology library followed by a colon (:). If you have multiple libraries loaded in memory with the same name, you must specify the file name.

library

The name of a library in memory, followed by a slash (/).

cell

The name of a library cell.

pin

The name of a cell's pin.

For example, to set the dont_use attribute on the AND4 cell in the my_lib library, enter

```
dc_shell> set_dont_use my_lib/AND4
```

To set the disable_timing attribute on the Z pin of the AND4 cell in the my_lib library, enter one of the following commands (depending on your shell mode):

```
dc_shell> set_disable_timing find(pin, my_lib/AND4/Z)
dc_shell-t> set_disable_timing [get_pins my_lib/AND4/Z]
```

Directing Library Cell Usage

When Design Compiler maps a design to a technology library, it selects components (library cells) from that library. You can influence the choice of components (library cells) by

- Excluding cells from the target library
- Specifying cell preferences

Excluding Cells From the Target Library

Use the set_dont_use command to exclude cells from the target library. Design Compiler does not use these excluded cells during optimization.

This command affects only the copy of the library that is currently loaded into memory and has no effect on the version that exists on disk. However, if you save the library, the exclusions are saved and the cells are permanently disabled.

For example, to prevent Design Compiler from using the high-drive inverter INV_HD, enter

```
dc_shell> set_dont_use MY_LIB/INV_HD
Performing set_dont_use on library cell 'MY_LIB/INV_HD'.
1
```

Use the `remove_attribute` command to reinclude excluded cells in the target library.

```
dc_shell> remove_attribute MY_LIB/INV_HD dont_use
Performing remove_attribute on library cell 'MY_LIB/INV_HD'.
1
```

Specifying Cell Preferences

Use the `set_prefer` command to indicate preferred cells. You can issue this command with or without the `-min` option.

Use the command without the `-min` option if you want Design Compiler to prefer certain cells during the initial mapping of the design.

- Set the preferred attribute on particular cells to override the default cell identified by the library analysis step. This step occurs at the start of compilation to identify the starting cell size for the initial mapping.
- Set the preferred attribute on cells if you know the preferred starting size of the complex cells or the cells with complex timing arcs (such as memories and banked components).

You do not normally need to set the preferred attribute as part of your regular compile methodology because a good starting cell is automatically determined during the library analysis step.

Because nonpreferred gates can be chosen to meet optimization constraints, the effect of preferred attributes might not be noticeable after optimization.

For example, to set a preference for the low-drive inverter INV_LD, enter

```
dc_shell> set_prefer MY_LIB/INV_LD
Performing set_prefer on library cell 'MY_LIB/INV_LD'.
1
```

Use the `remove_attribute` command to remove cell preferences.

```
dc_shell> remove_attribute MY_LIB/INV_LD preferred
Performing remove_attribute on library cell 'MY_LIB/INV_LD'.
1
```

Use the `-min` option if you want Design Compiler to prefer fewer (but larger-area) buffers or inverters when it fixes hold-time violations. Normally, Design Compiler gives preference to smaller cell area over the number of cells used in a chain of buffers or inverters. You can change this preference by using the `-min` option, which tells Design Compiler to minimize the number of buffers or inverters by using larger area cells.

For example, to set a `hold_preferred` attribute for the inverter IV, enter

```
dc_shell> set_prefer -min class/IV
Performing set_prefer on library cell 'class/IV'.
1
```

Use the `remove_attribute` command to remove the `hold_preferred` cell attribute.

```
dc_shell> remove_attribute class/IV hold_preferred
Performing remove_attribute on library cell 'class/IV'.
{"class/IV"}
```

Removing Libraries From Memory

The `remove_design` command removes libraries from dc_shell memory. If you have multiple libraries with the same name loaded into memory, you must specify the path as well as the library name. Use the `list -libraries` command to see the path for each library in memory (dcsh mode only).

Saving Libraries

The `write_lib` command saves (writes to disk) a compiled library in Synopsys database, EDIF, or VHDL format.

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UNITED STATES DISTRICT COURT
NORTHERN DISTRICT OF CALIFORNIA

RICOH COMPANY, LTD.,

Plaintiff,

vs.

AEROFLEX ET AL,

Defendants.

CASE NO. CV 03-4669-MJJ (EMC)

Consolidated with

CASE NO. CV 03-2289

NOTICE OF MANUAL FILING

SYNOPSYS, INC.,

Plaintiff,

vs.

RICOH COMPANY, LTD.,

Defendants.

Please take notice that Plaintiff Ricoh Company, Ltd., is filing the following documents on this date in paper form only:

1. Ricoh's Opposition to Defendants' Motion for Partial Summary Judgment.
2. Deposition transcript of Edward Dwyer of February 3, 2004 (Exhibit 7 to the Declaration of Michael Weinstein in Support of Ricoh's Opposition to Defendants' Motion for Partial Summary Judgment).
3. Chip Synthesis Workshop – Lab Guide (Exhibit 14 to the Declaration of Michael Weinstein in Support of Ricoh's Opposition to Defendants' Motion for Partial Summary Judgment).

Because the above documents include and refer to materials produced in discovery and designated confidential by the ASIC Defendants and Synopsys, a request to file these documents under seal will be filed contemporaneously.

Dated: August 23, 2005

Respectfully submitted,

Ricoh Company, Ltd.

By: /s/ Kenneth W. Brothers

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PROOF OF SERVICE

CASE: *Ricoh Company, Ltd. v. Aeroflex Incorporated, et al.*
Synopsys, Inc. v. Ricoh Company, Ltd.

CASE NOS.: U.S. District Court, N.D. Cal., Nos. C03-4669 and C03-2289 MJJ

I am employed in the City and County of San Francisco, California. I am over the age of eighteen years and not a party to the within action; my business address is 177 Post Street, Suite 300, San Francisco, California 94108. On August 23, 2005, I served the following document(s):

Ricoh's Opposition to Motion for Partial Summary Judgment.

Deposition transcript of Edward Dwyer of February 3, 2004 (Exhibit 7 to the Declaration of Michael Weinstein in Support of Ricoh's Opposition to Defendants' Motion for Partial Summary Judgment).

Chip Synthesis Workshop - Lab Guide (Exhibit 14 to the Declaration of Michael Weinstein in Support of Ricoh's Opposition to Defendants' Motion for Partial Summary Judgment).

on the parties, through their attorneys of record, by sending true copies thereof as shown below for service as designated below:

By Electronic Mail: I caused such document(s) to be served via electronic mail (email) on the parties in this action by transmitting a true copy to the following email address(es):

ADDRESSEE	PARTY
Teresa M. Corbin, Esq. Jaclyn Fink, Esq. Howrey Simon Arnold & White LLP 525 Market Street, Suite 3600 San Francisco, CA 94105-2708 CorbinT@howrey.com finkj@howrey.com	Defendants

I declare under penalty of perjury under the laws of the State of California that the foregoing is true and correct. Executed this August 23, 2005, at San Francisco, California.

/s/
Edward Lin